COMPAL CONFIDENTIAL

MODEL(NA)ME: EDC42

PCB NO : LA-H27/1/R

BOM P/N:

GPIO MAP: X10_WHL_KBL_CFLH_GPIO map Rev1.5_20180921

PWR Circuit: 14UMA_A00_FWR_20190308A

Brook Hollow 14 UMA (TBT)

Cof f ee Lake H 2019-03-20

REV: 1.0 (A00)

@: Nopop Component

EMI@: EMI Component

@EMI@: EMI Nopop Component

ESD@: ESD Component

@ESD@: ESD Nopop Component

RF@: RF Component

@RF@: RF Nopop Component

XDP@: XDP Component

CONN@: Connector Component

5105@: EC MEC5105 IC

5106@: EC MEC5106 IC

WWAN@: WWAN Component

WWANRF@: WWAN RF Component

eSPI@:eSPI interface

LPC@: LPC interface

DS3@: Deep sleep support

NDS3@: non Deep sleep support

RTD3@: RTD3 support

NR703@: non RTD3 support

VPRO@:VPRO support

NVPRO@:non VPRO support

ST33@: ST33 TPM support

750@: NPCT7507PM support JUMP@: Jump solder and short

@JUMP@: Jump no solder/

SATAPERI@ : Pericom SATA repeater support

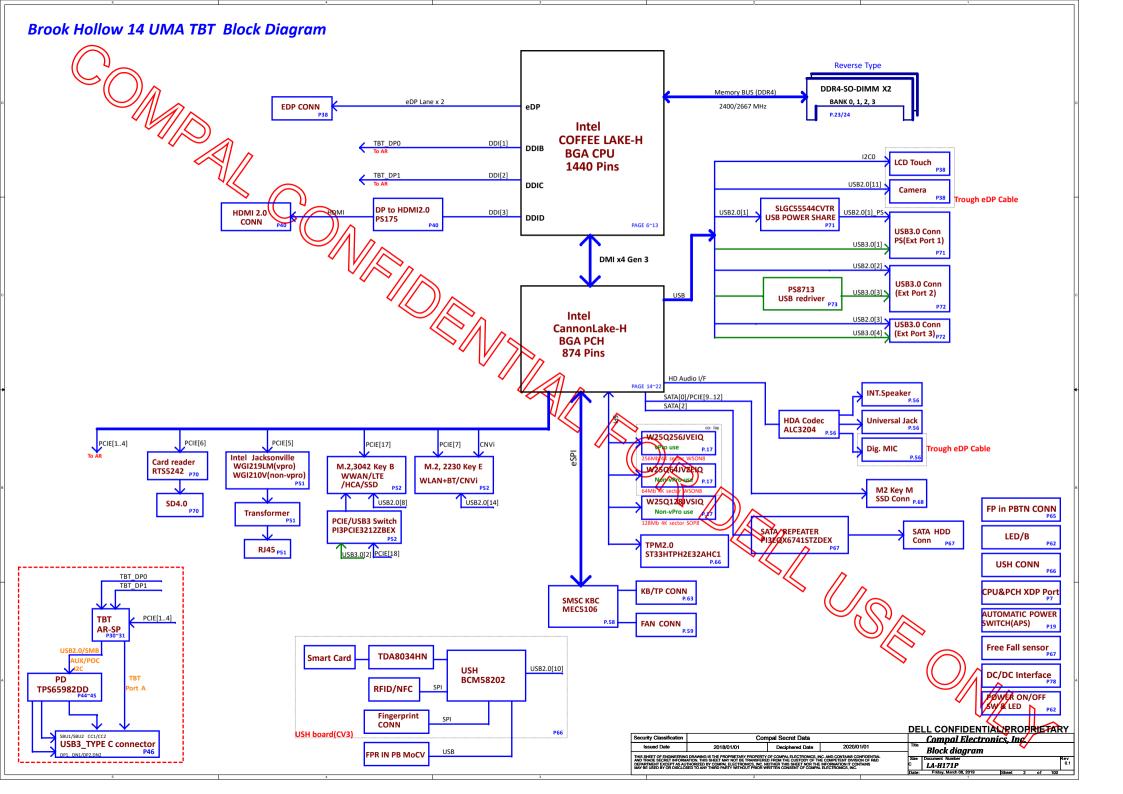
SATAPARA@: Parade SATA repeater support

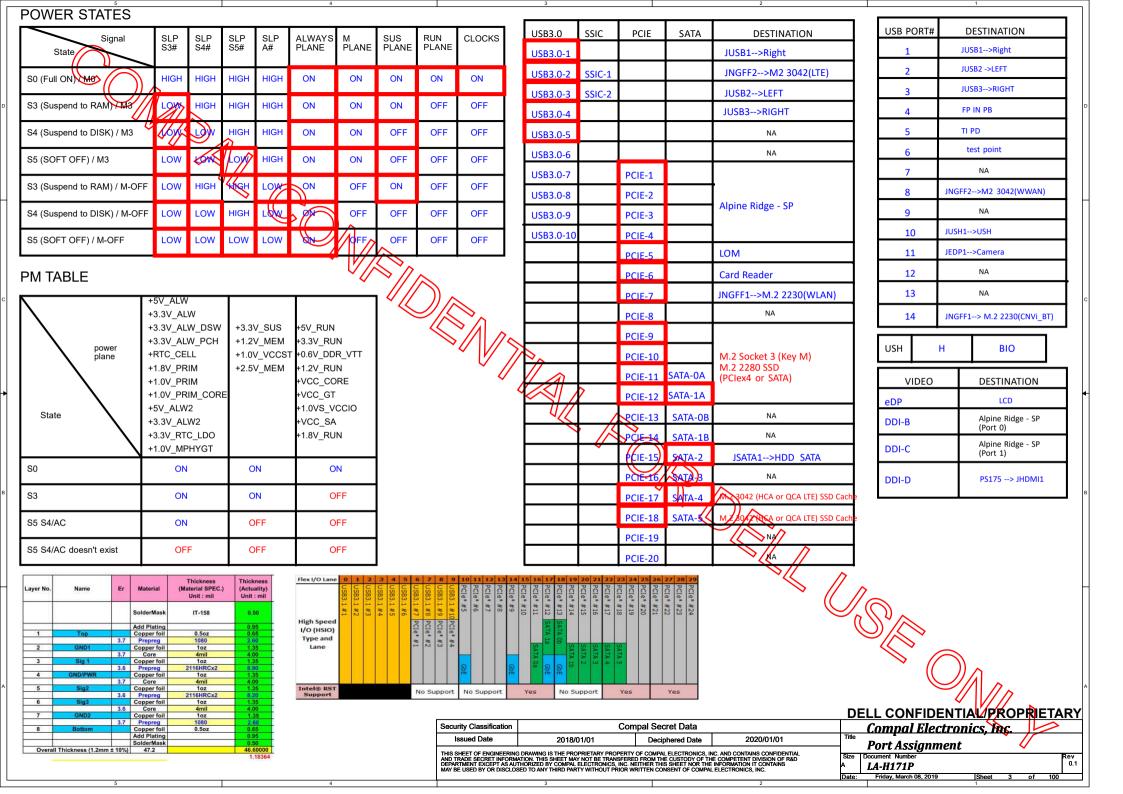
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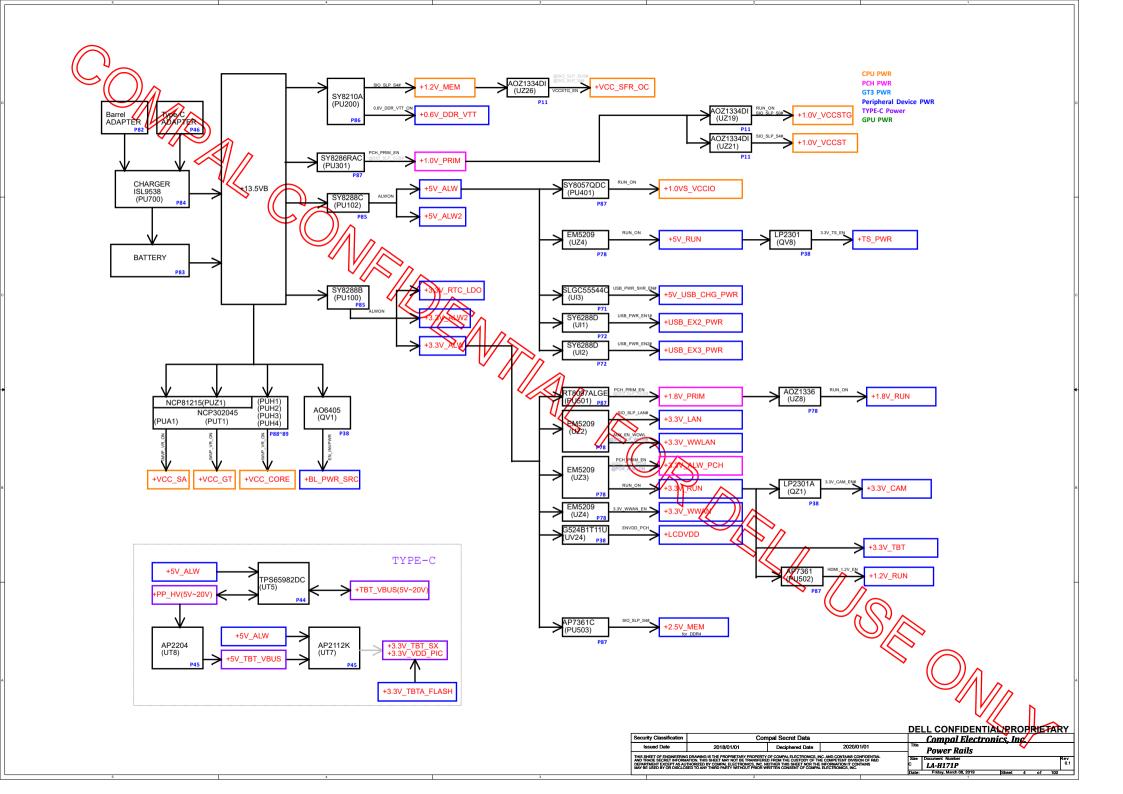


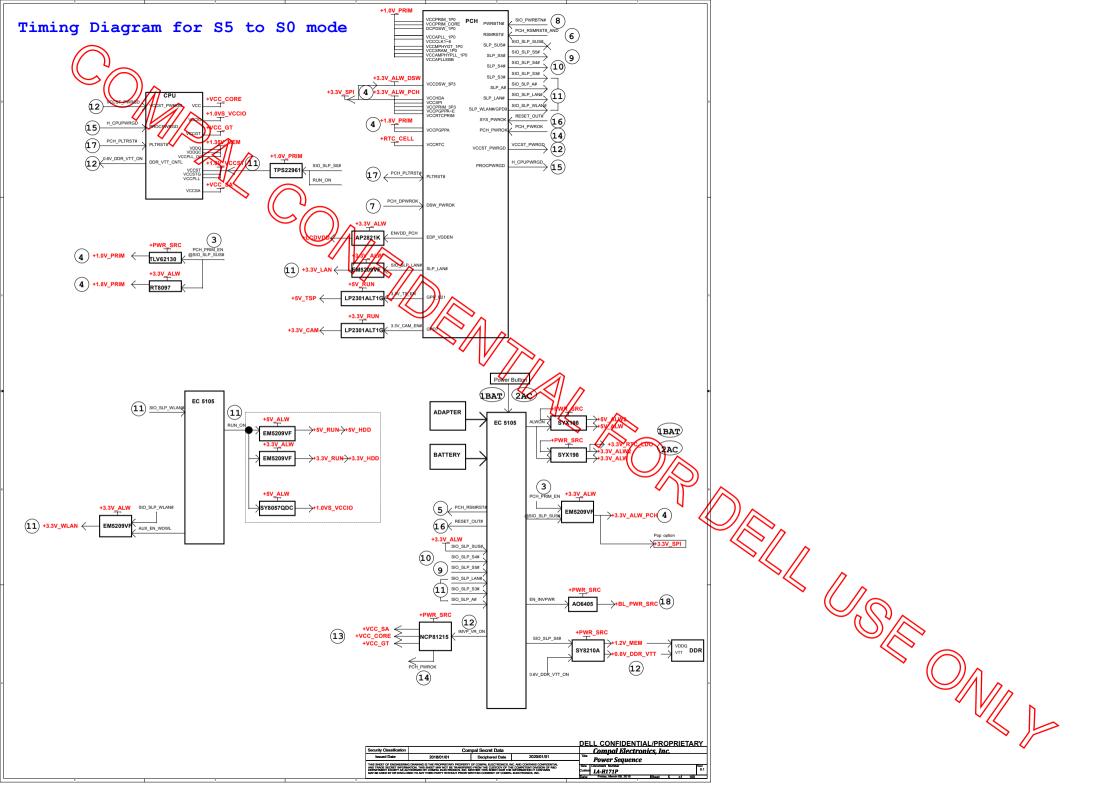
Layout Dell logo

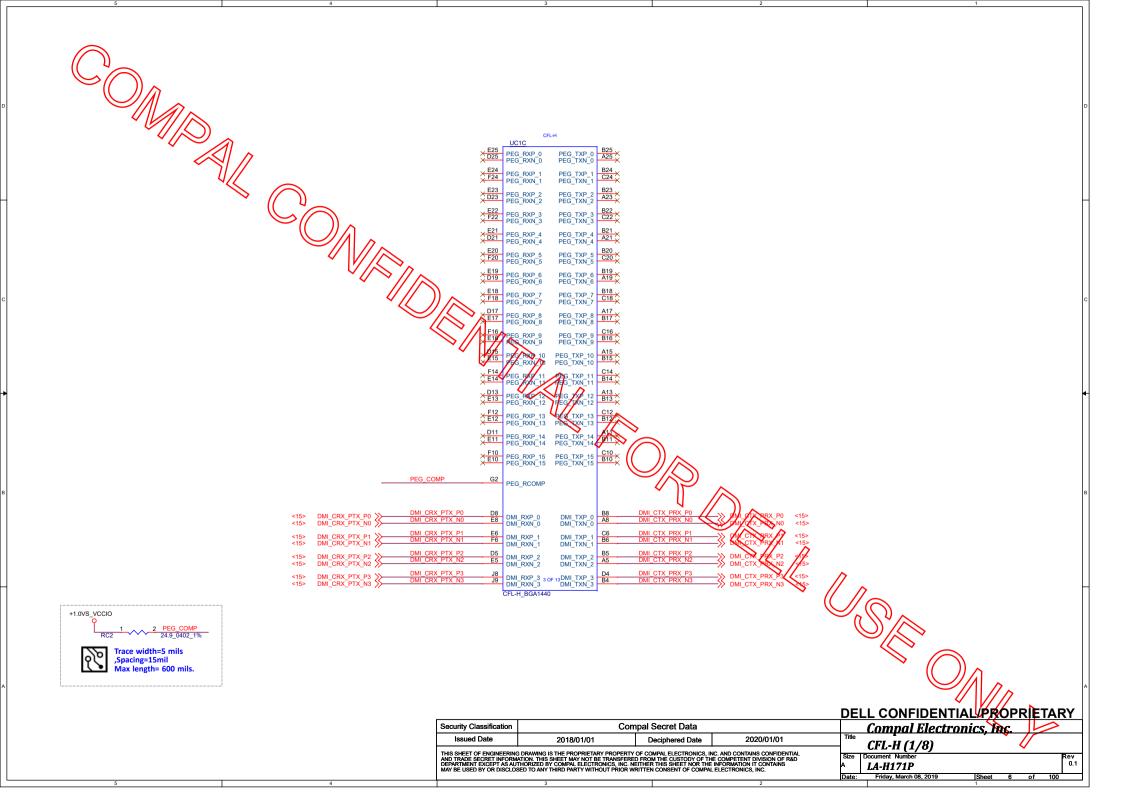
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REV: A00
PWB: J11RG

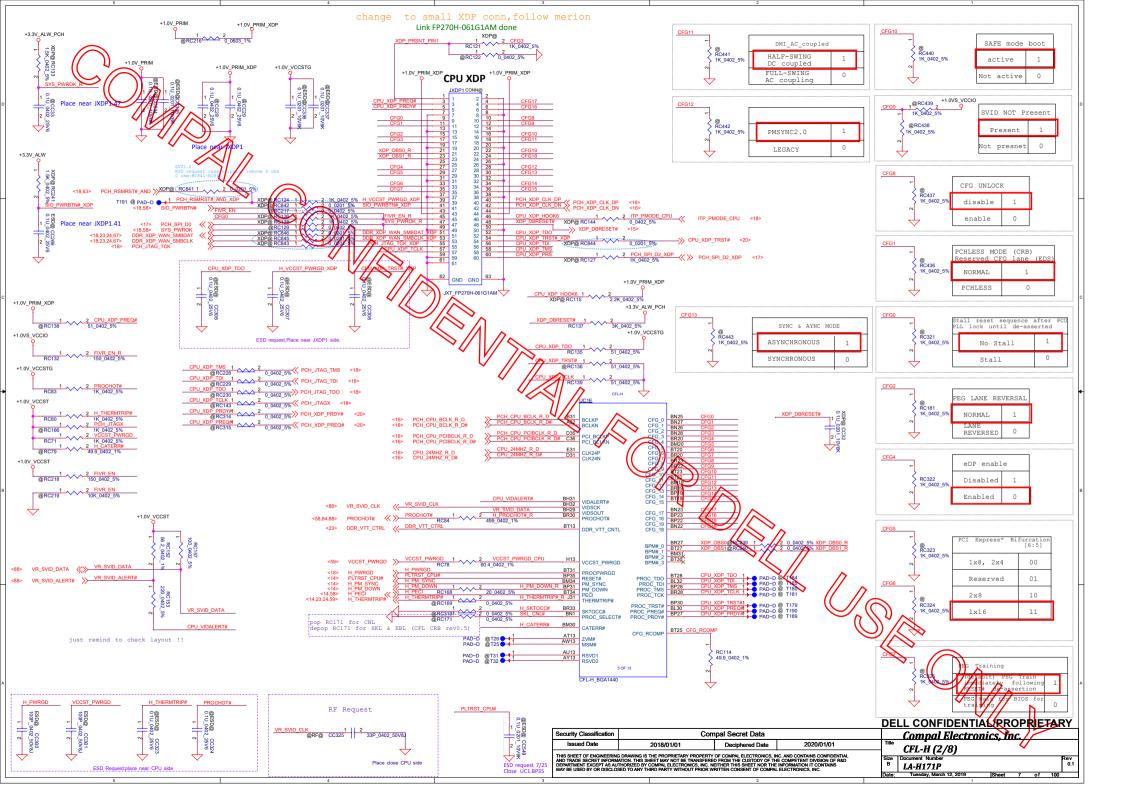


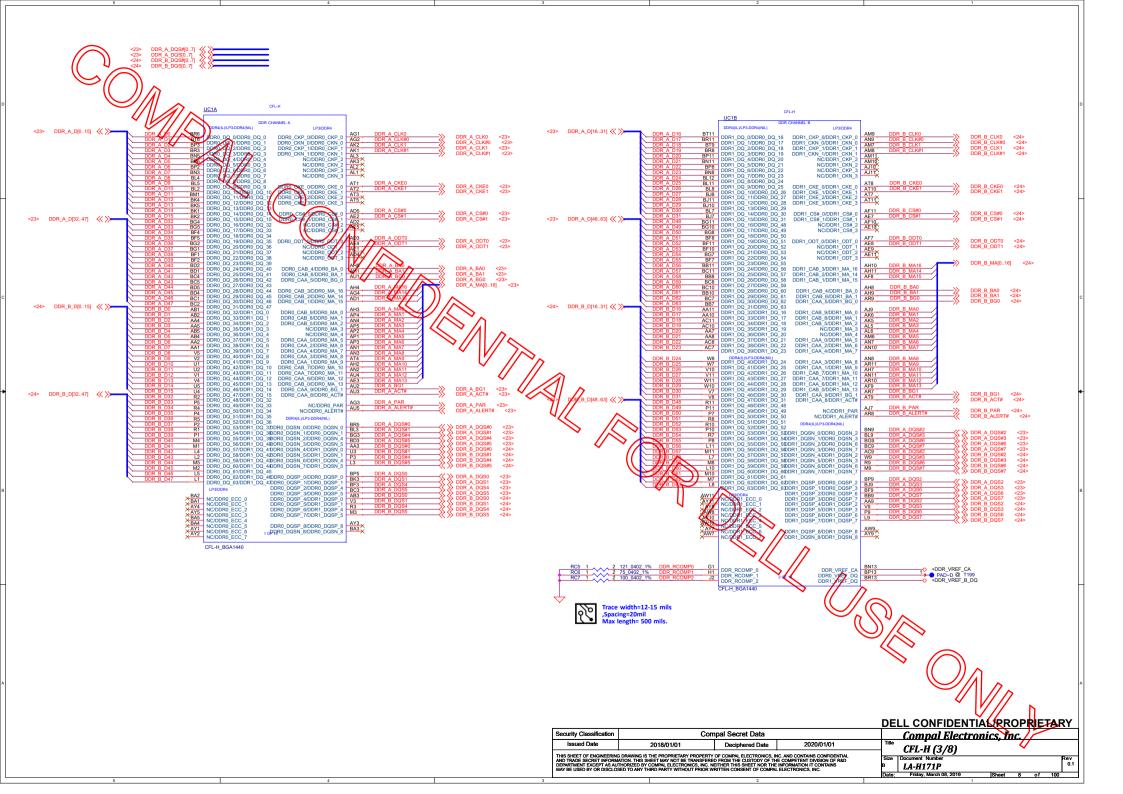


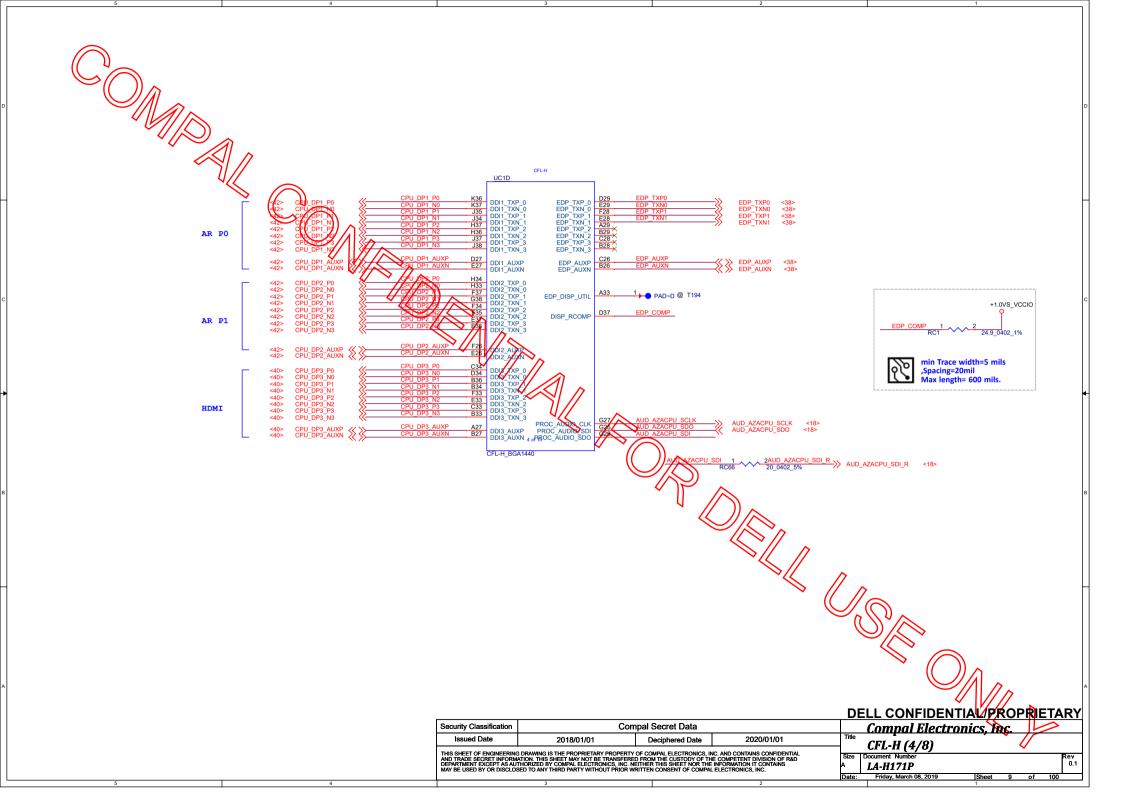


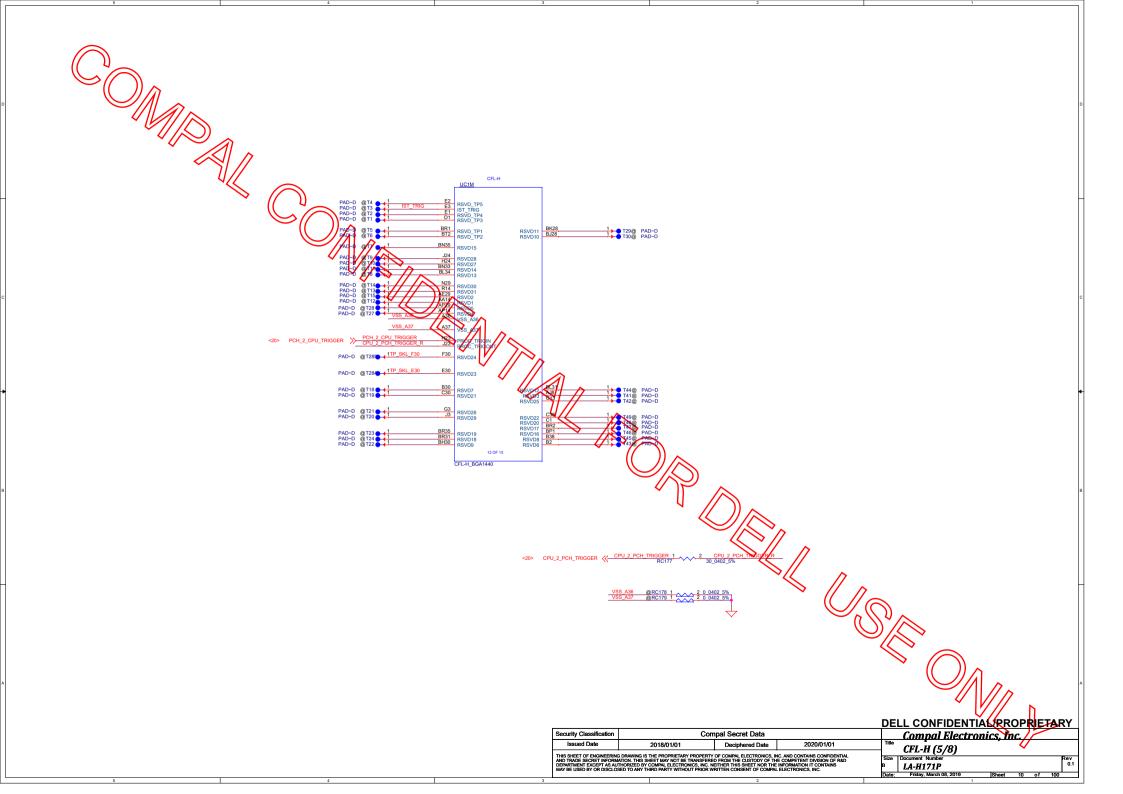


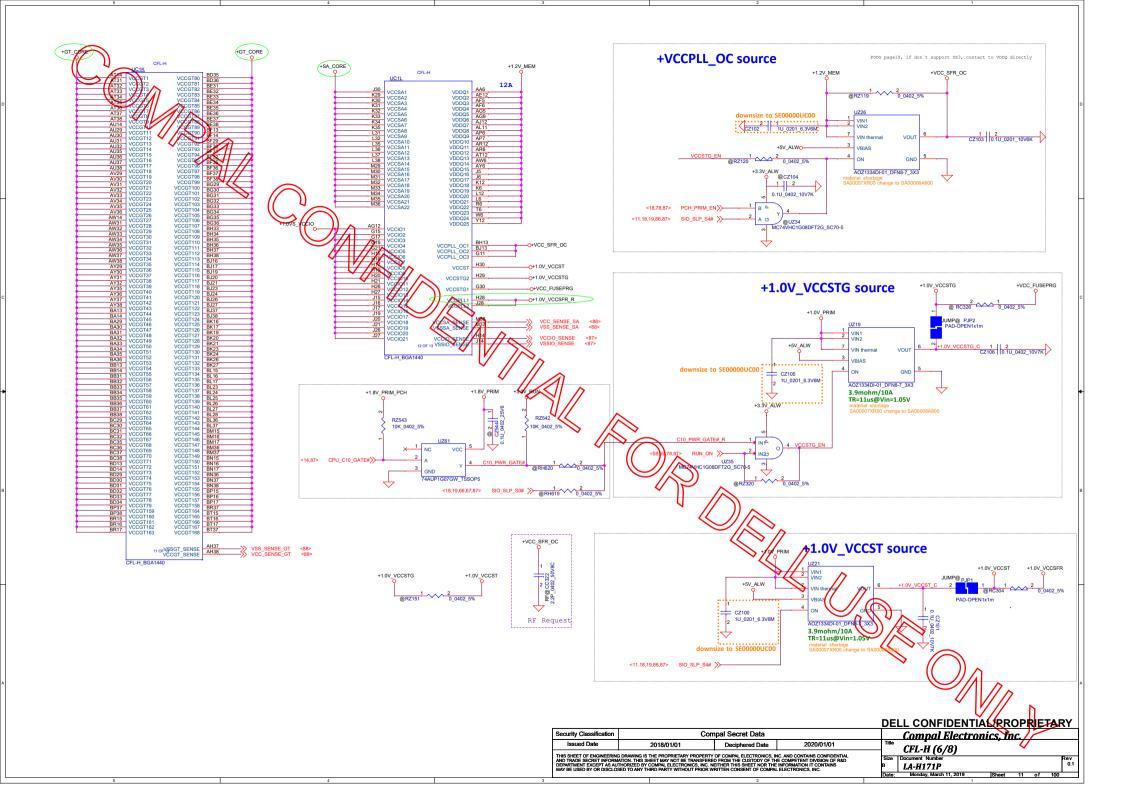


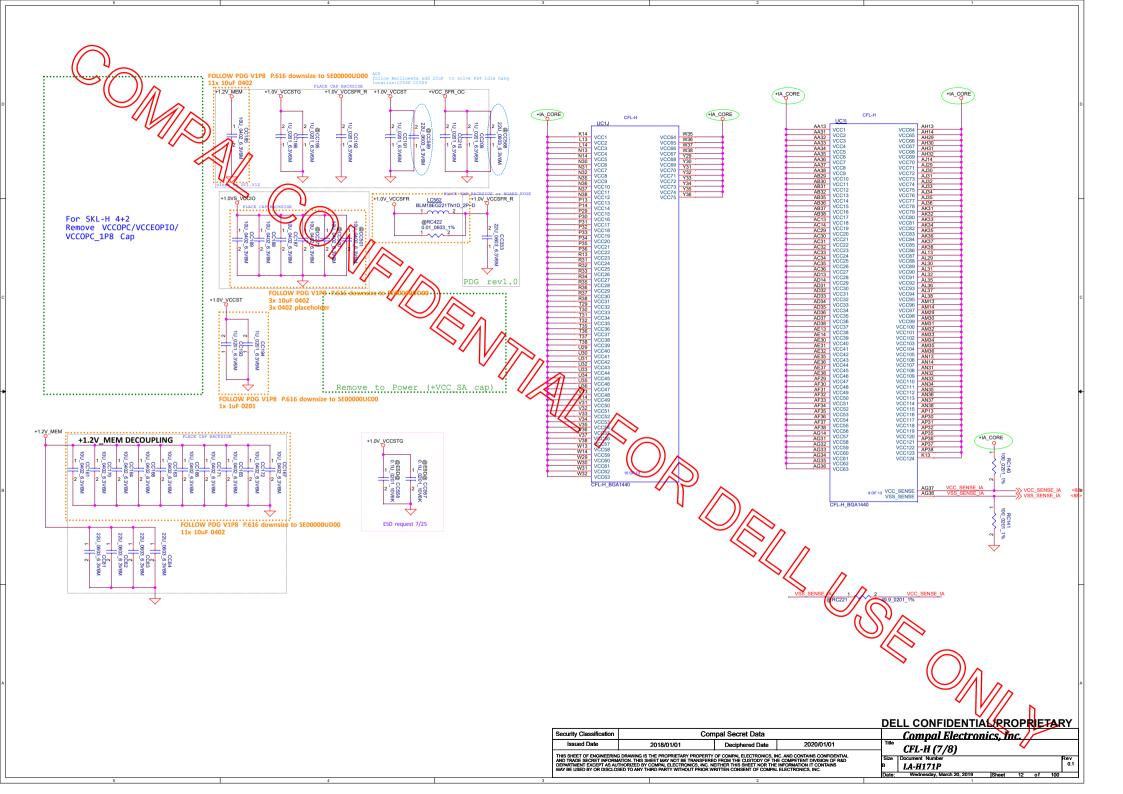




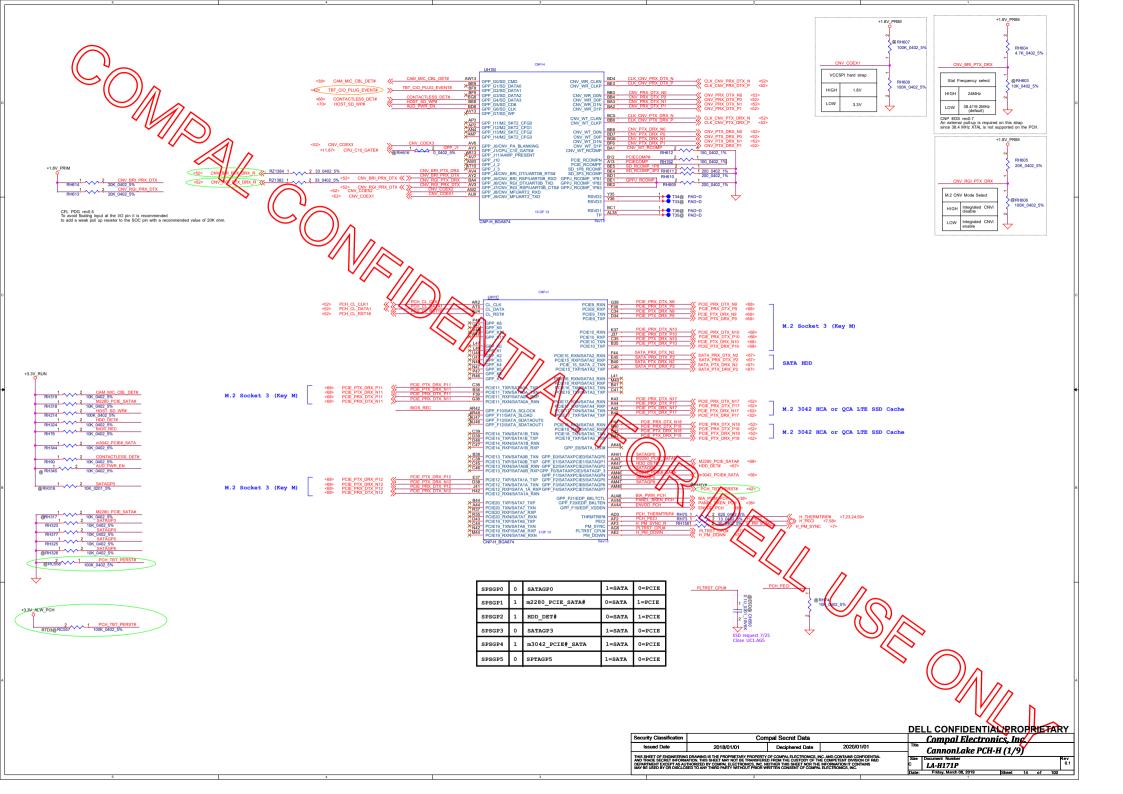


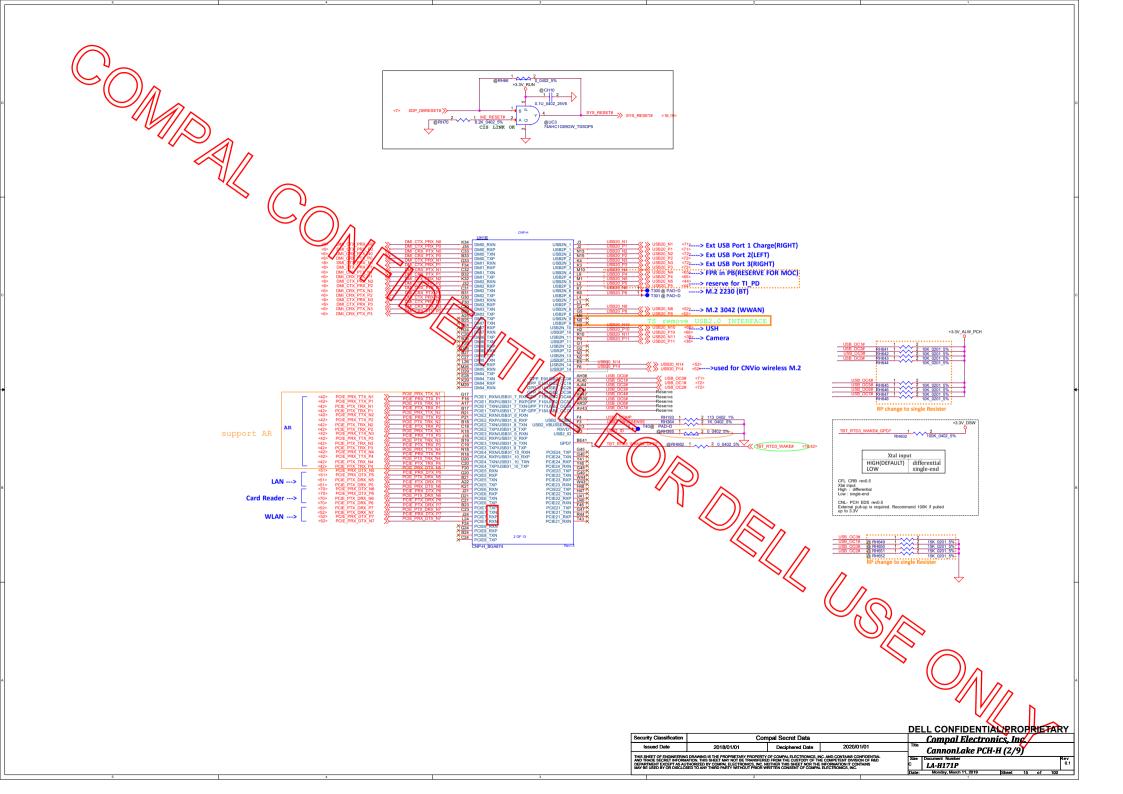


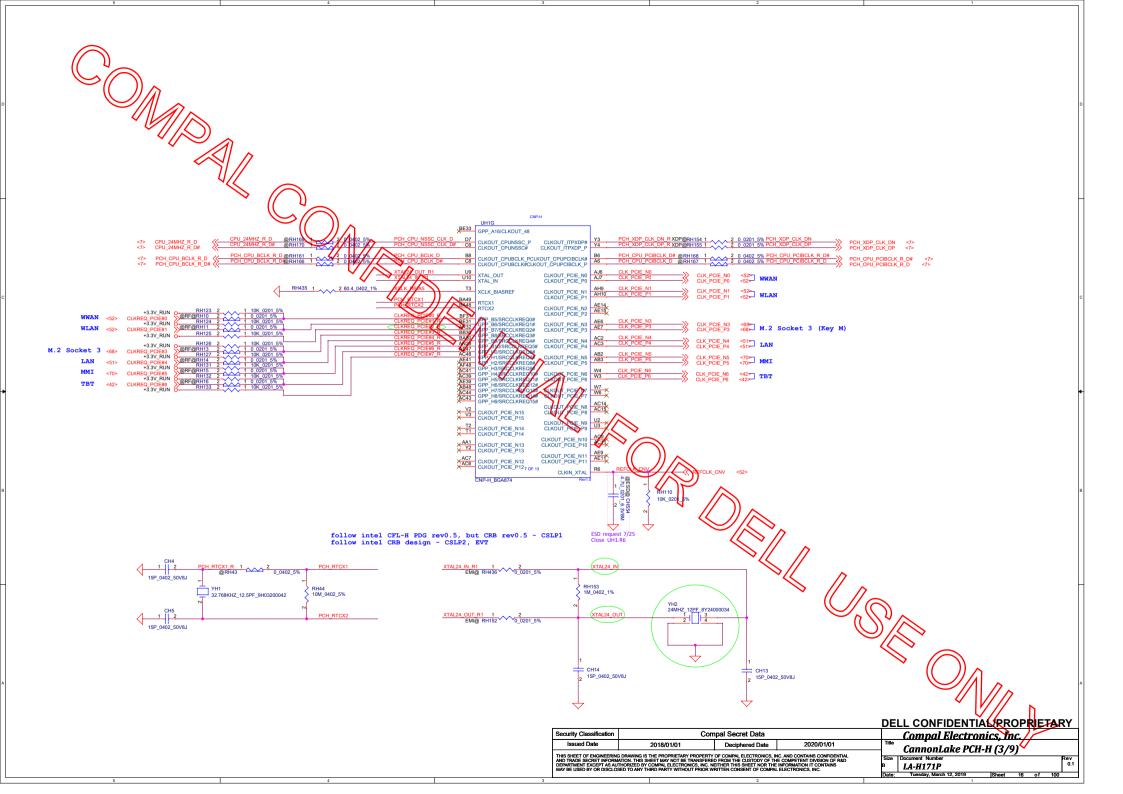


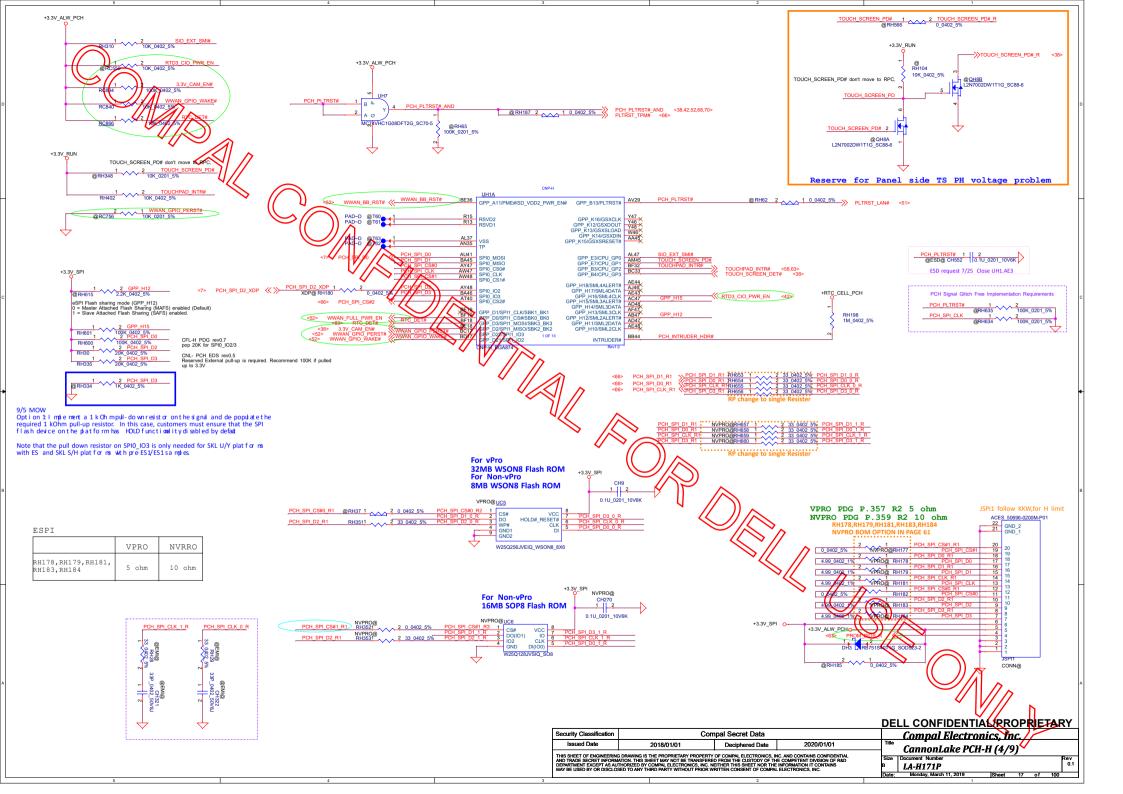


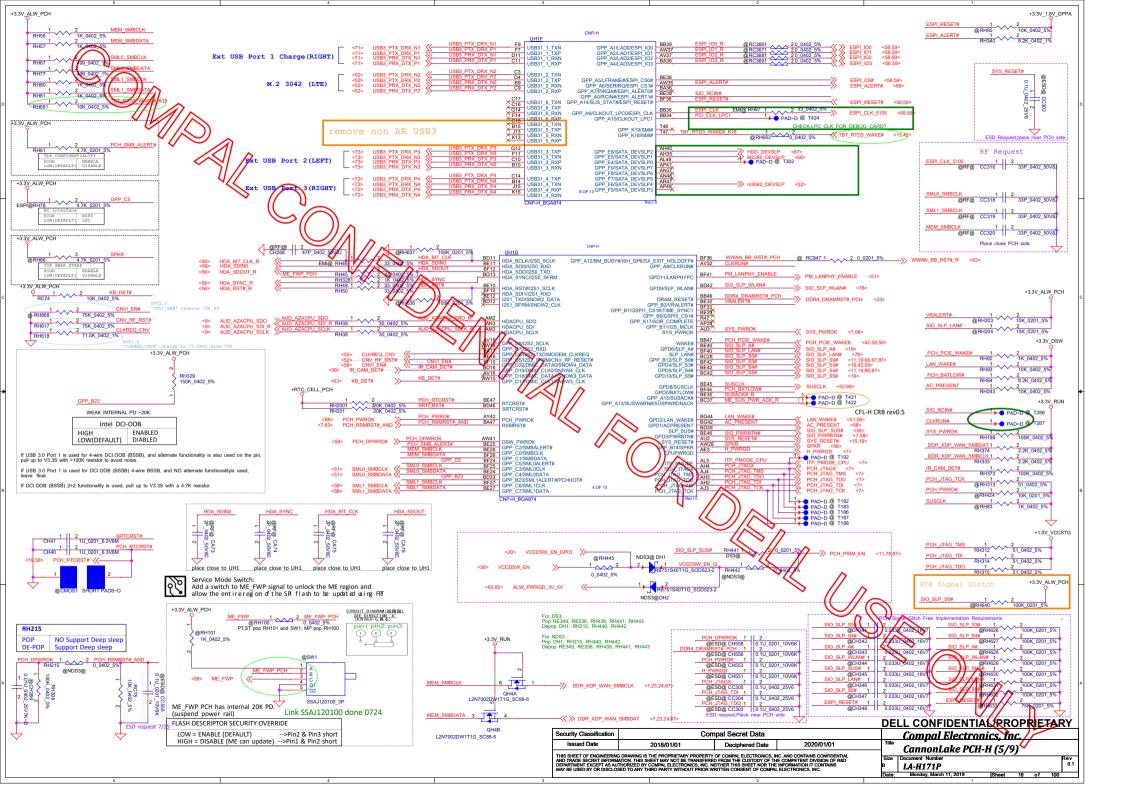


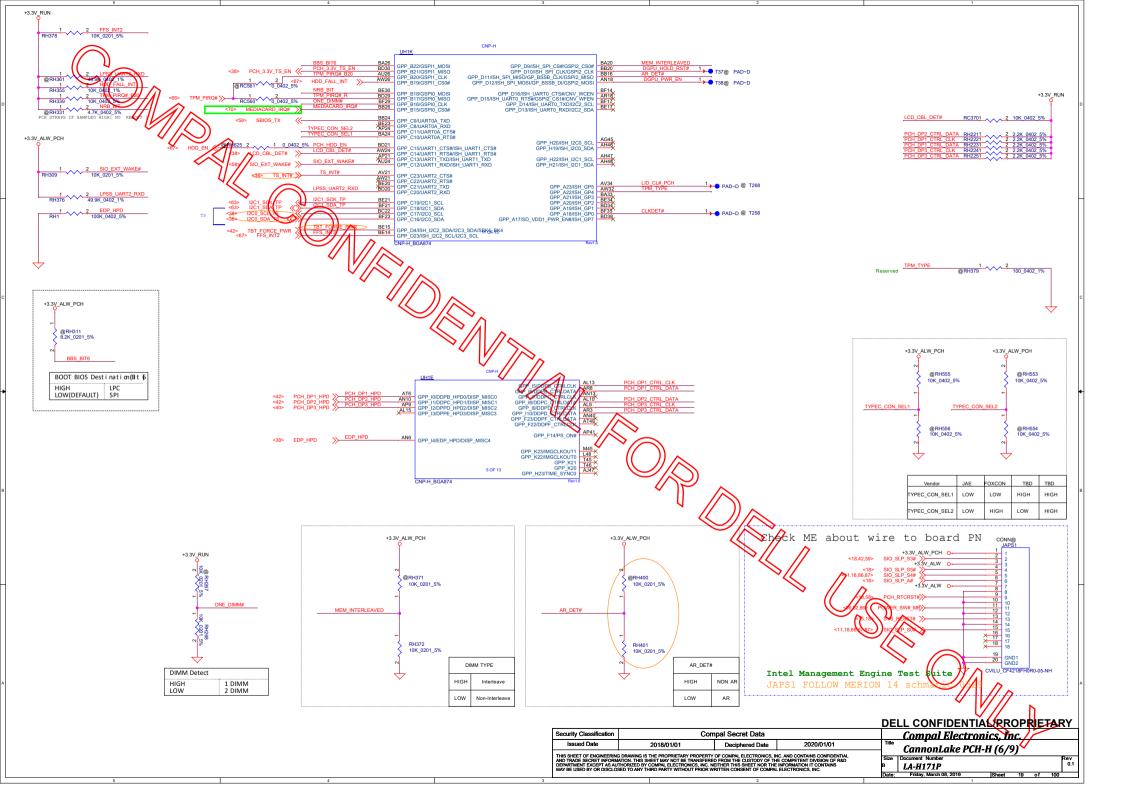


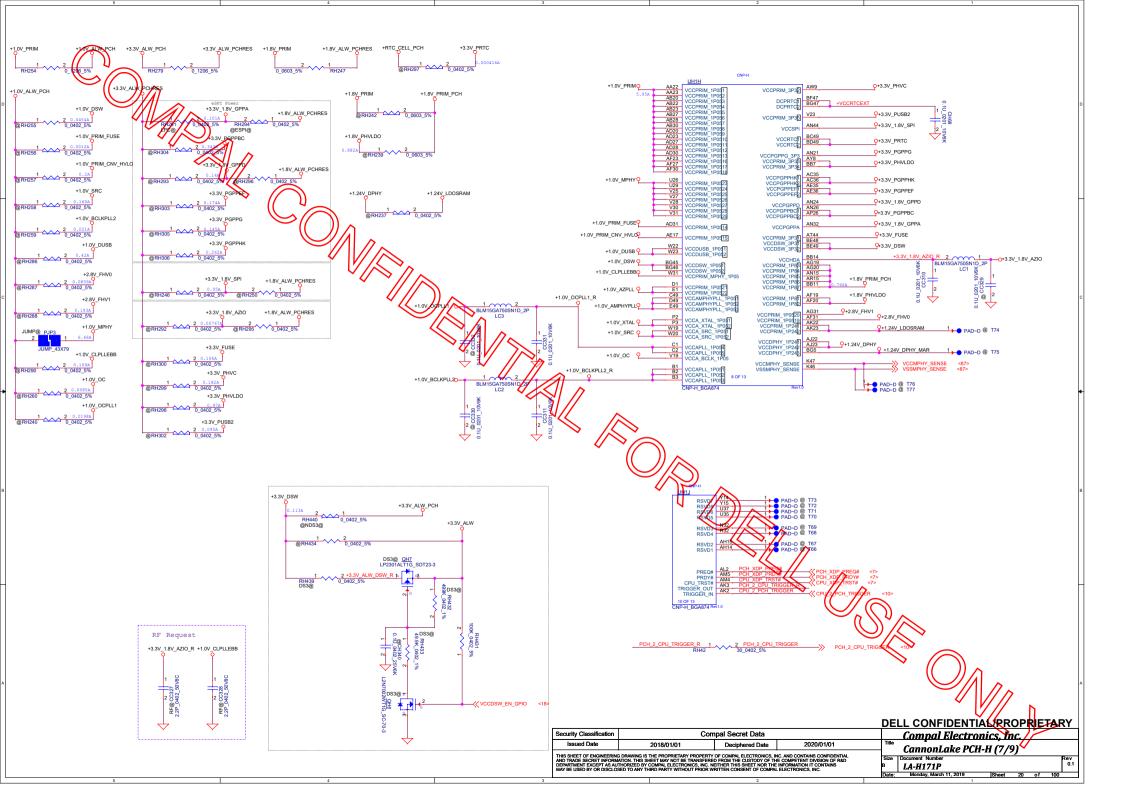


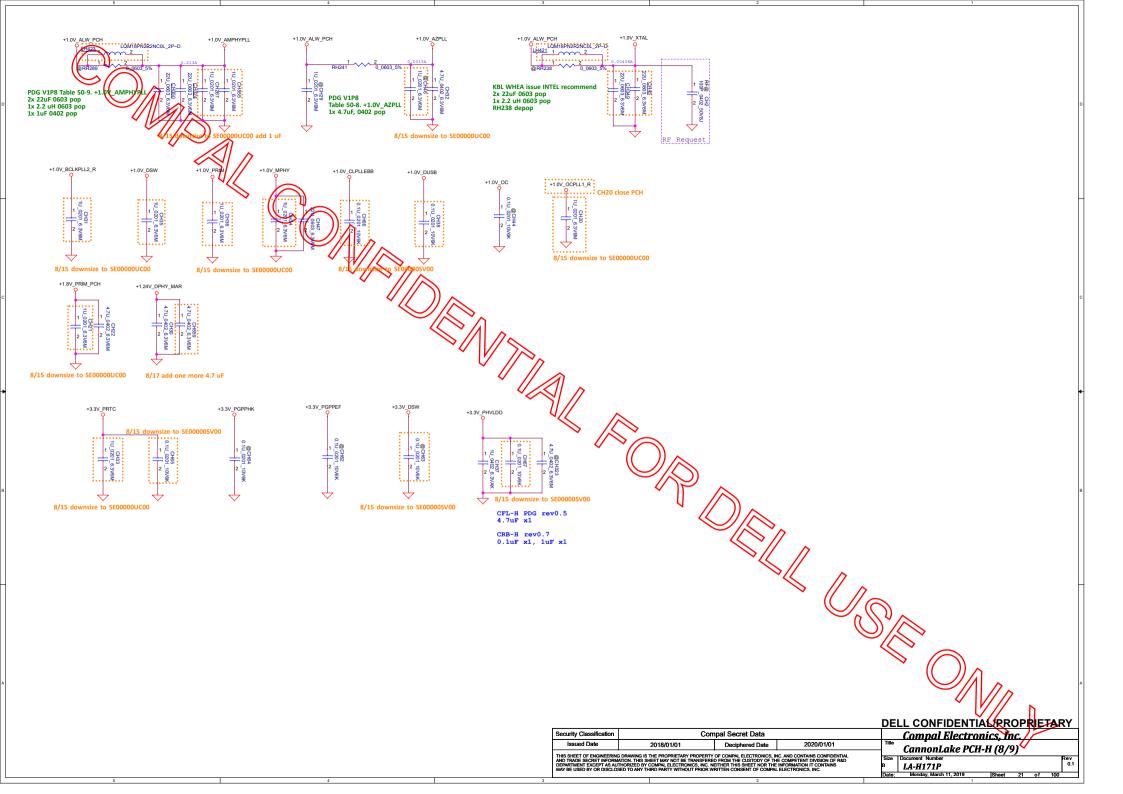




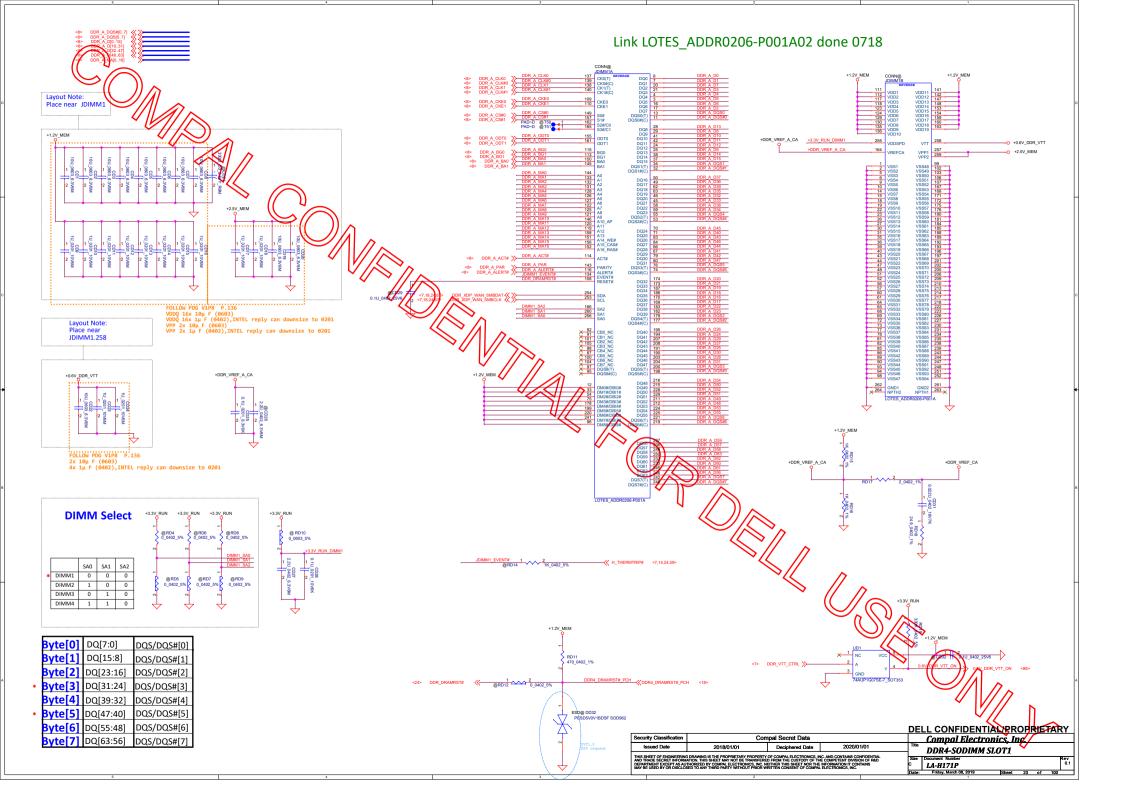


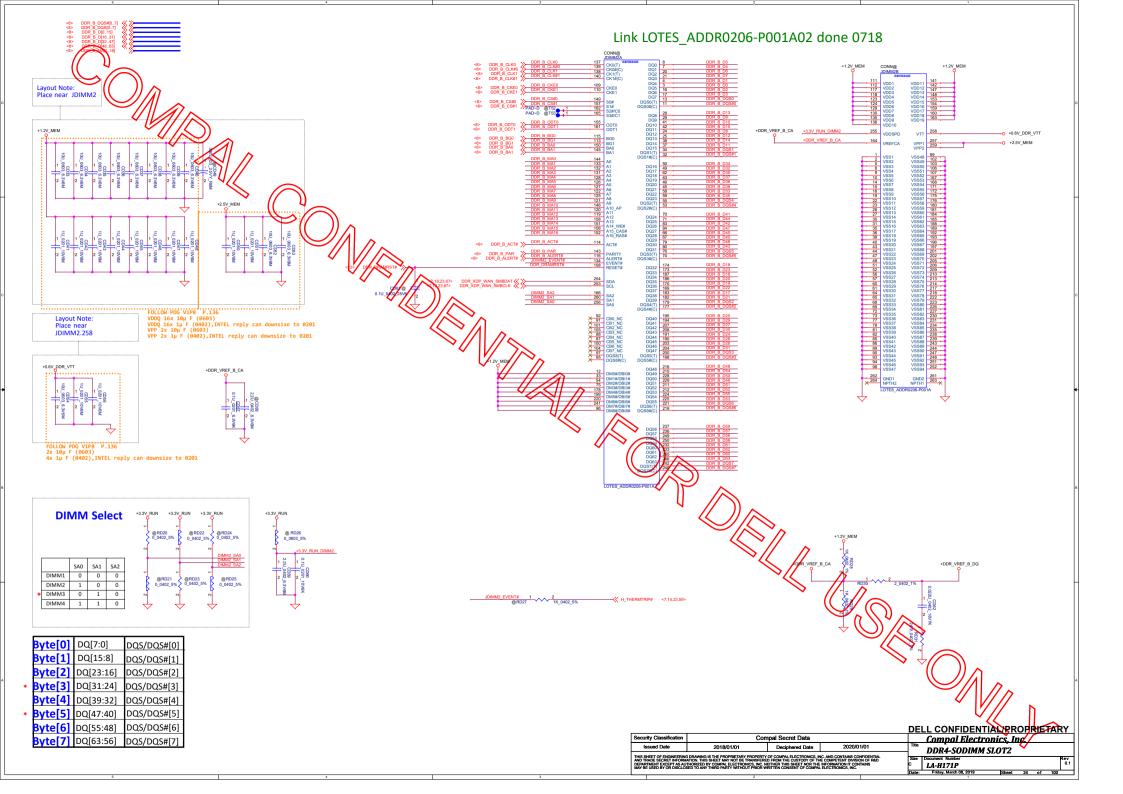




























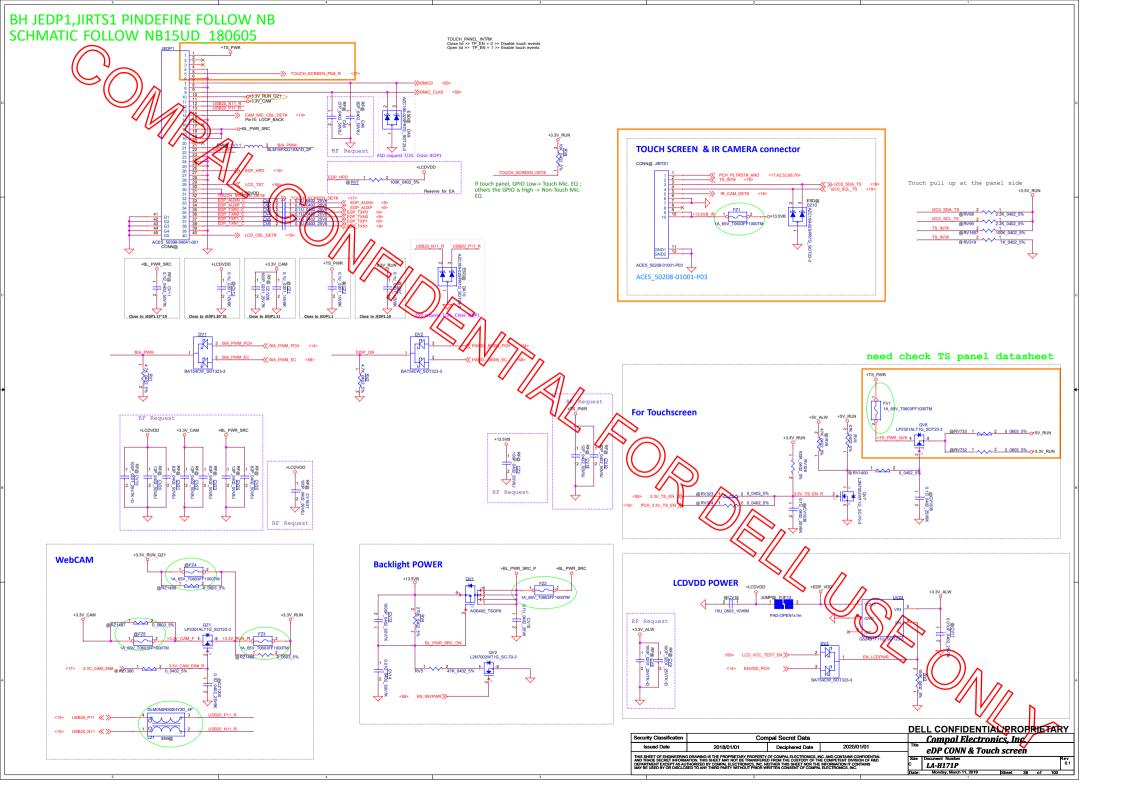




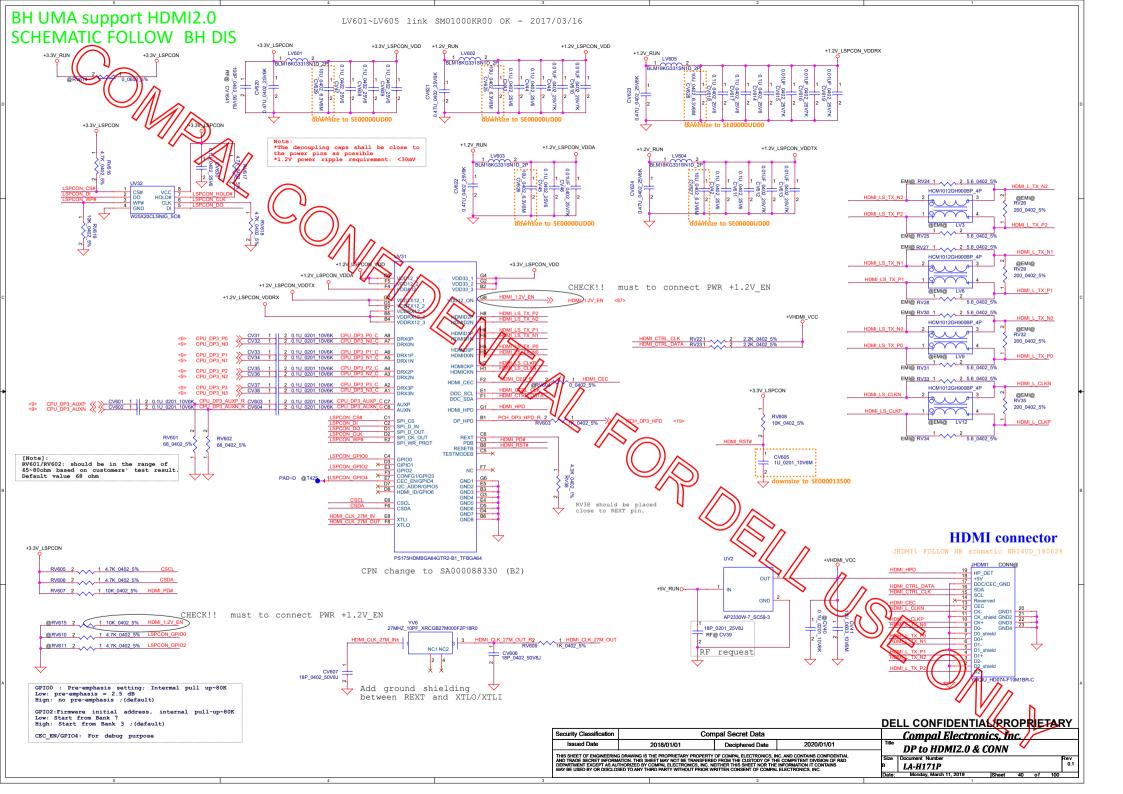




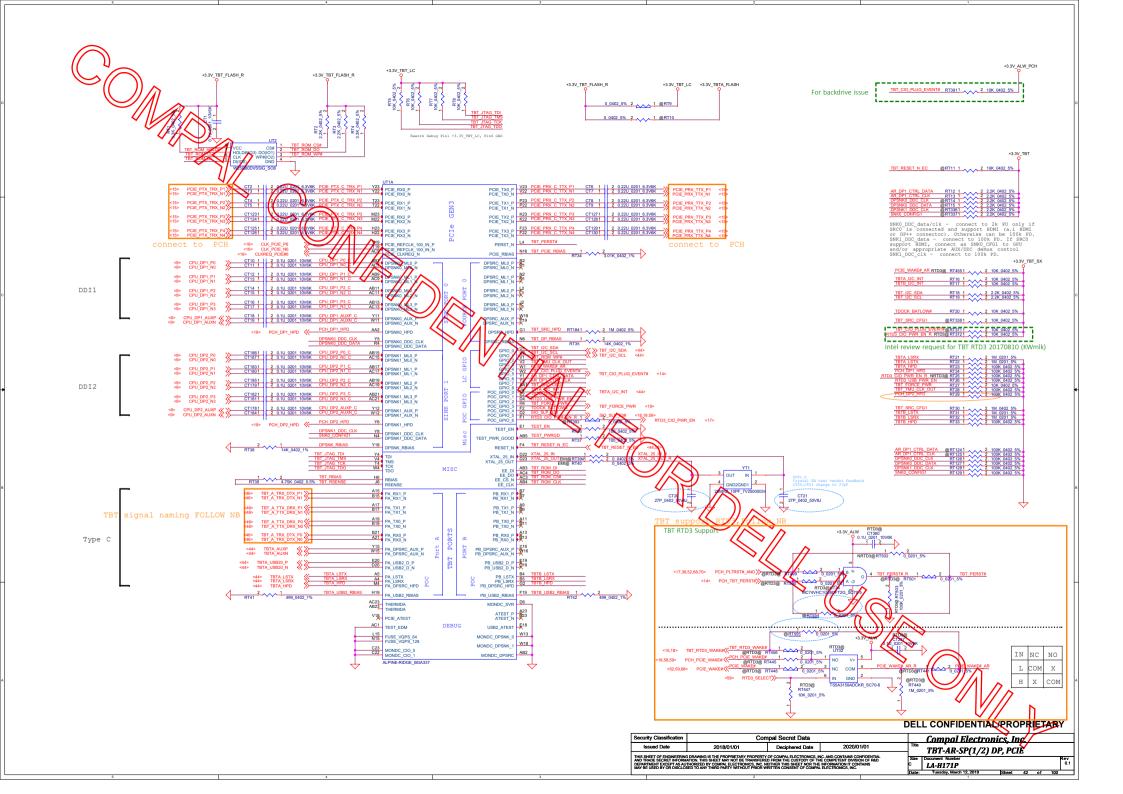


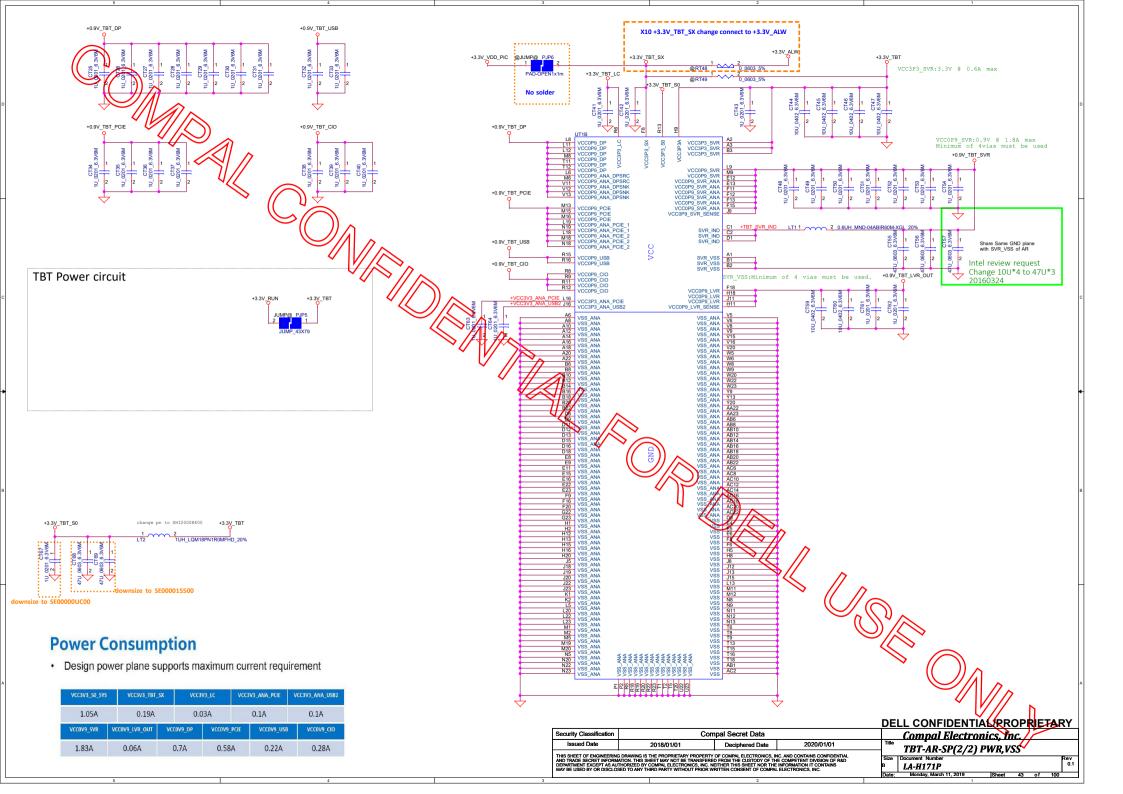


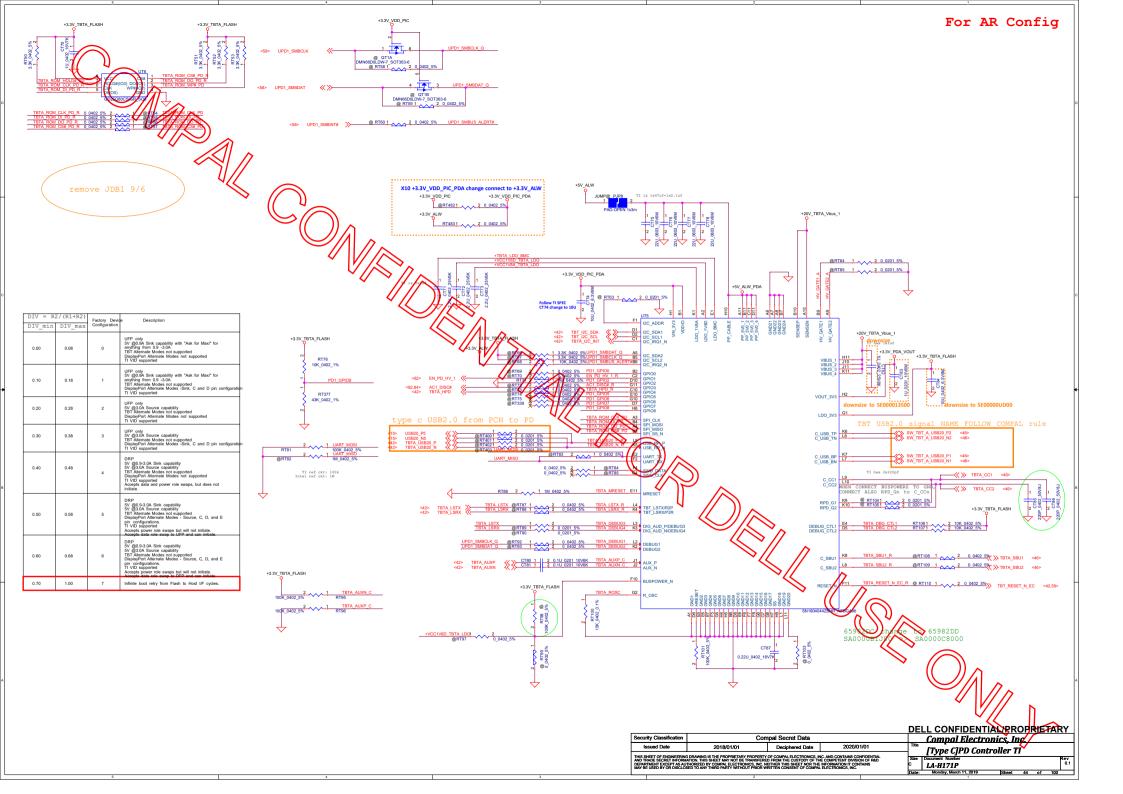


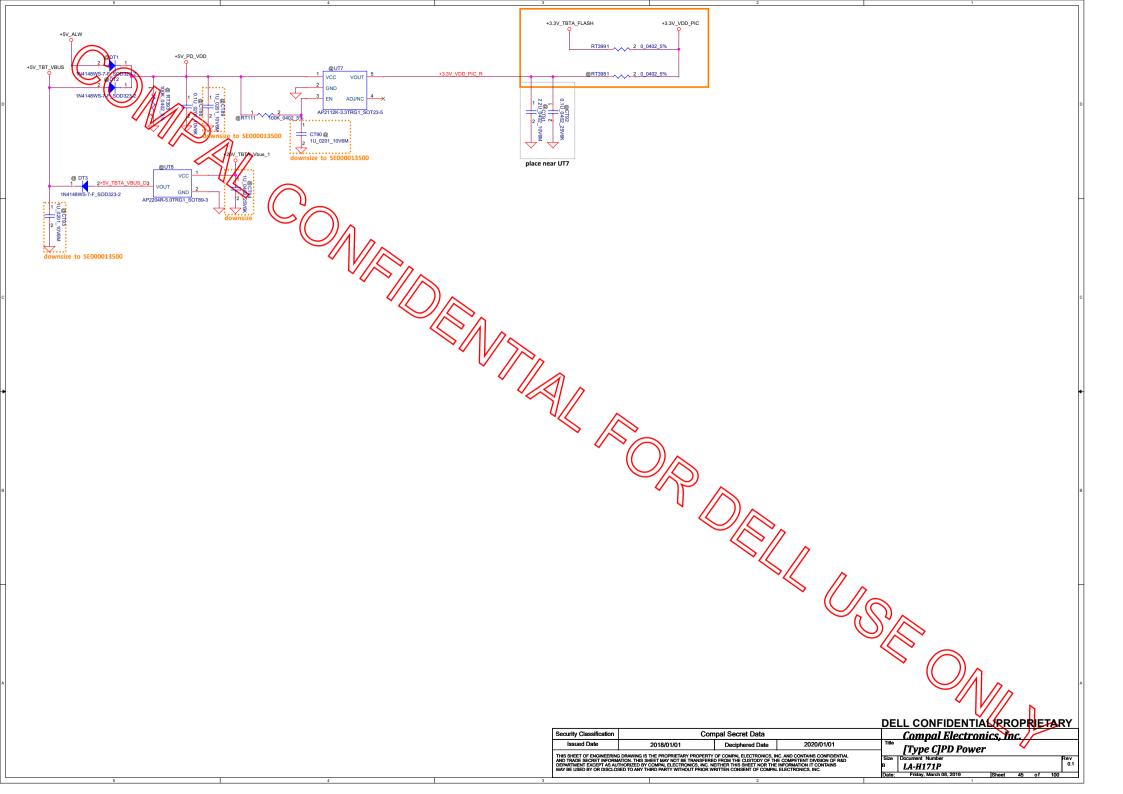


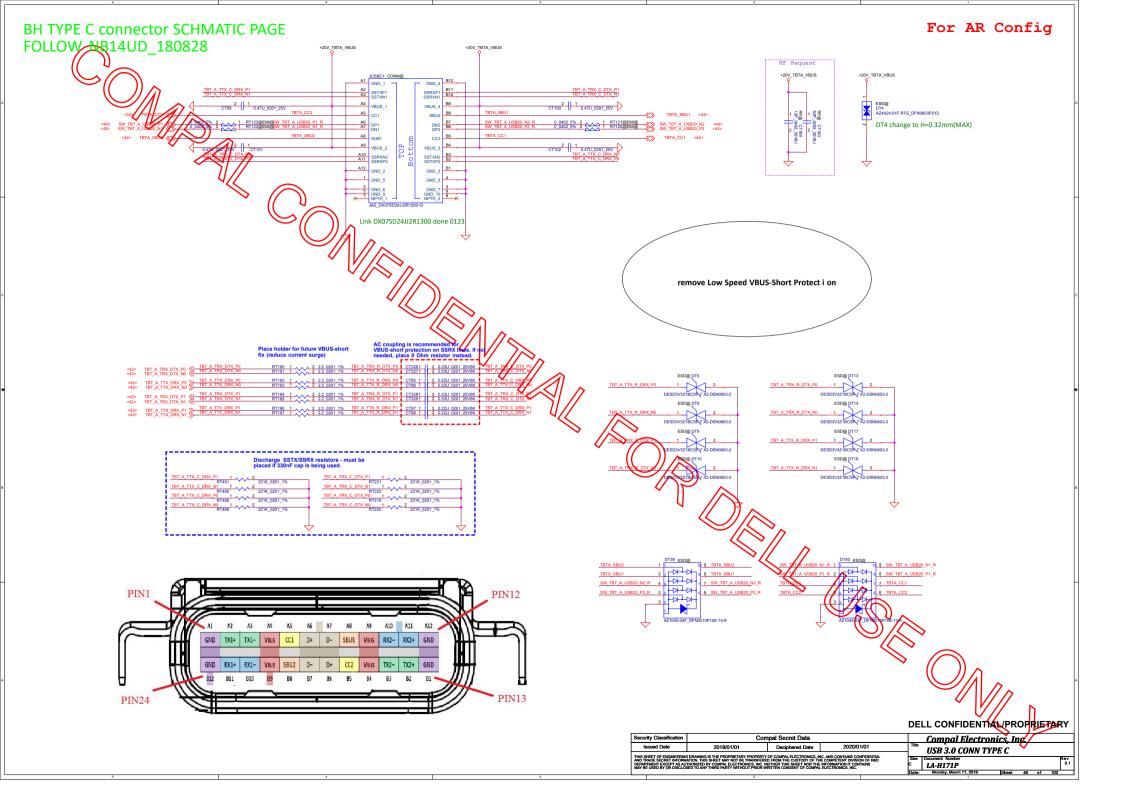


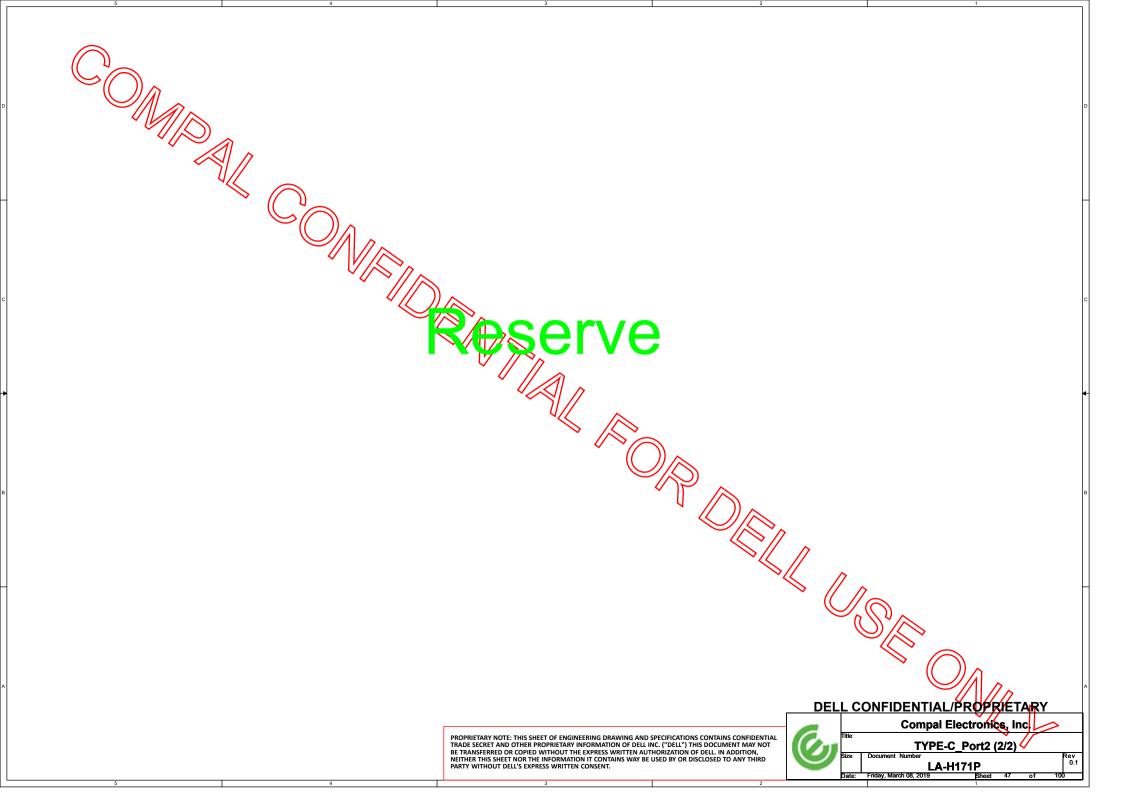








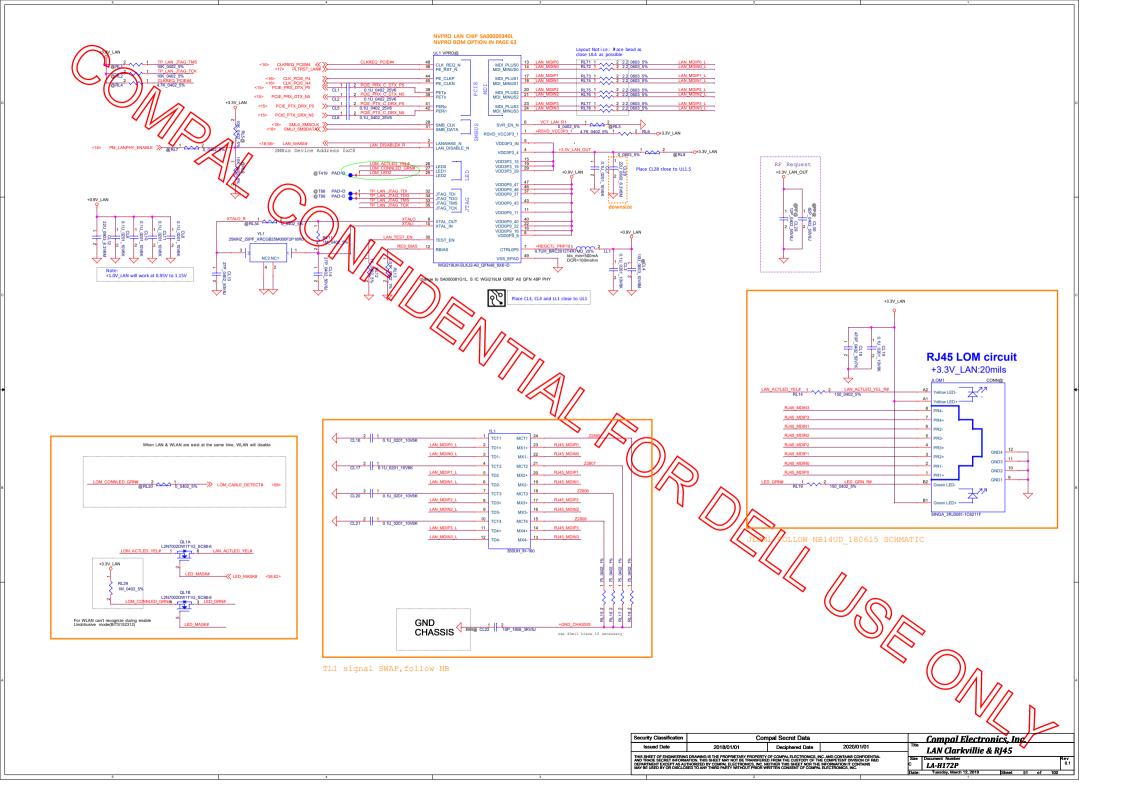


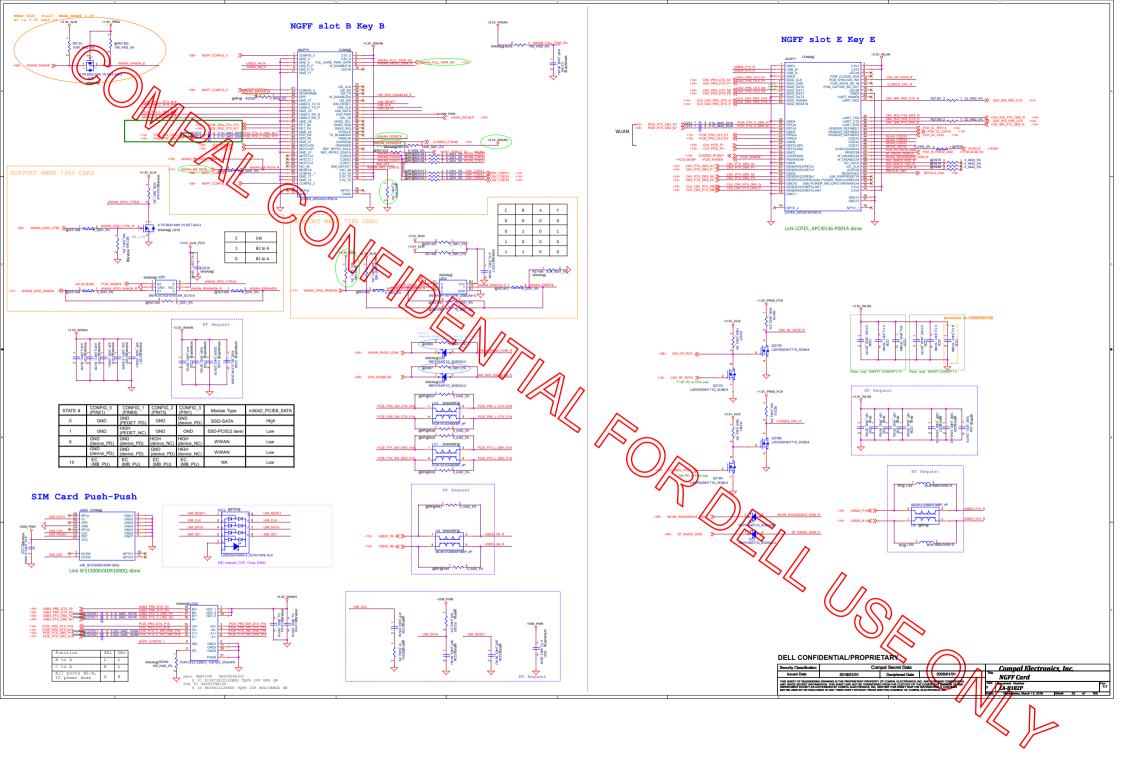








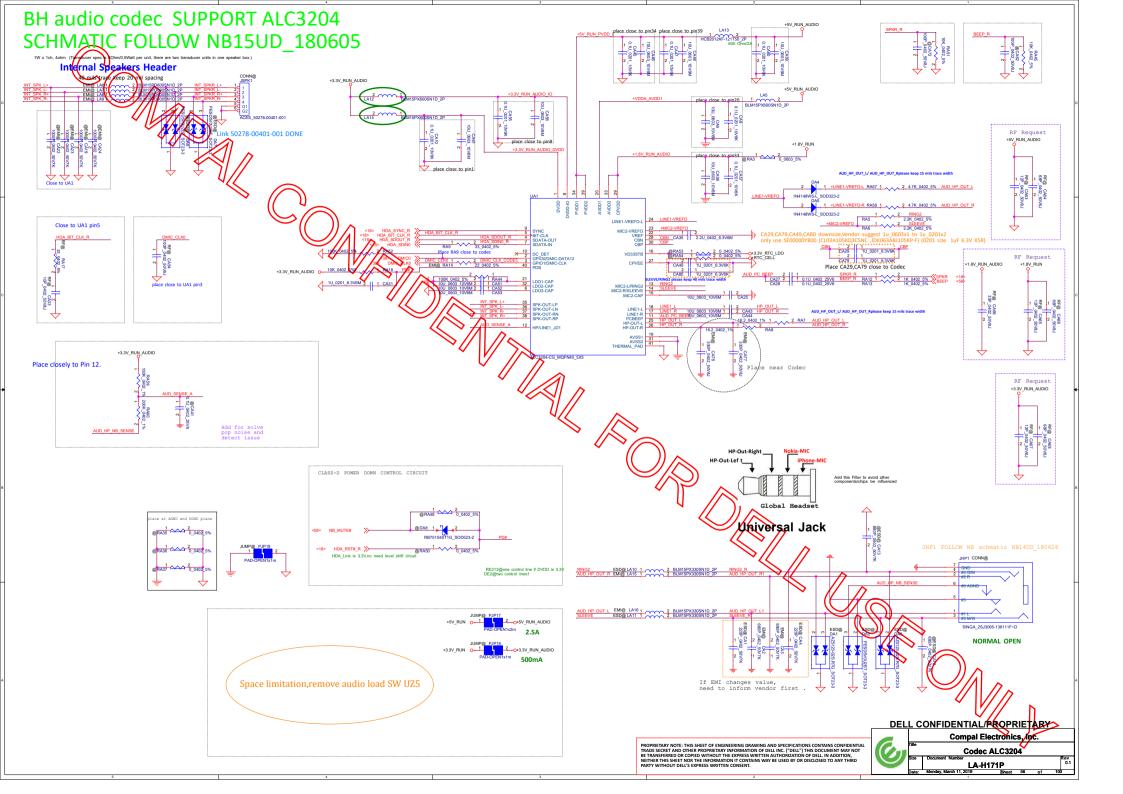




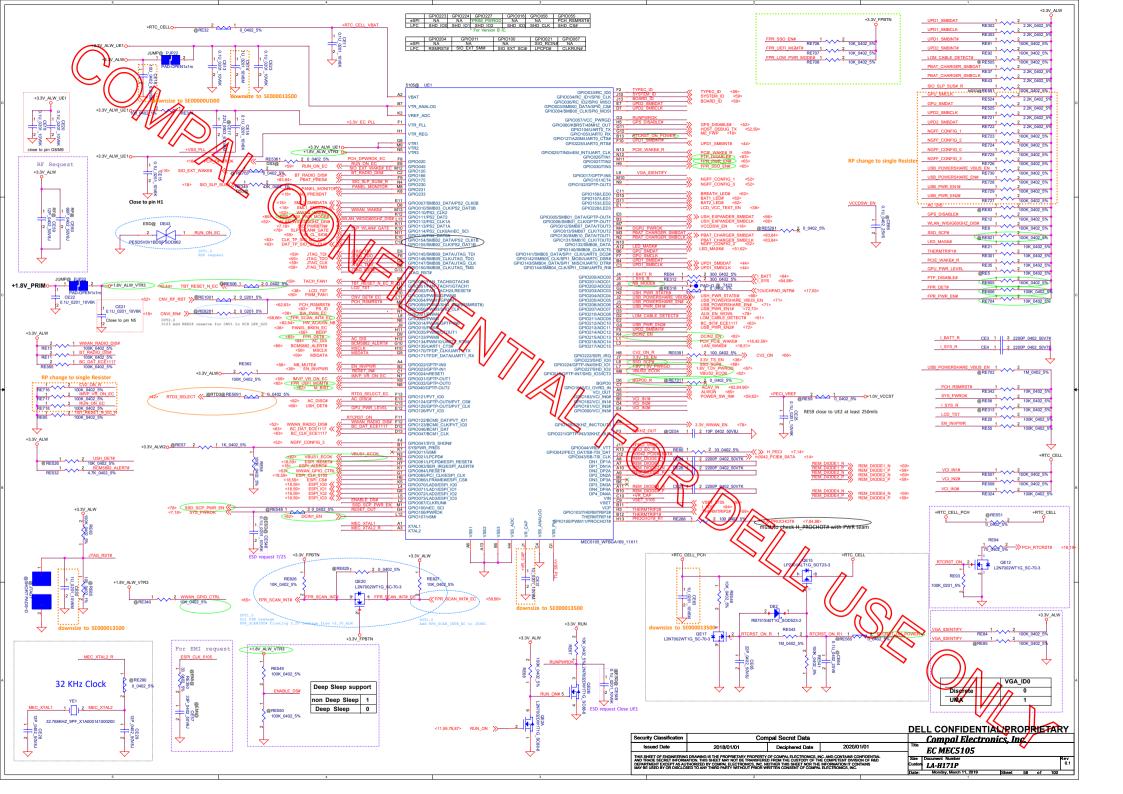


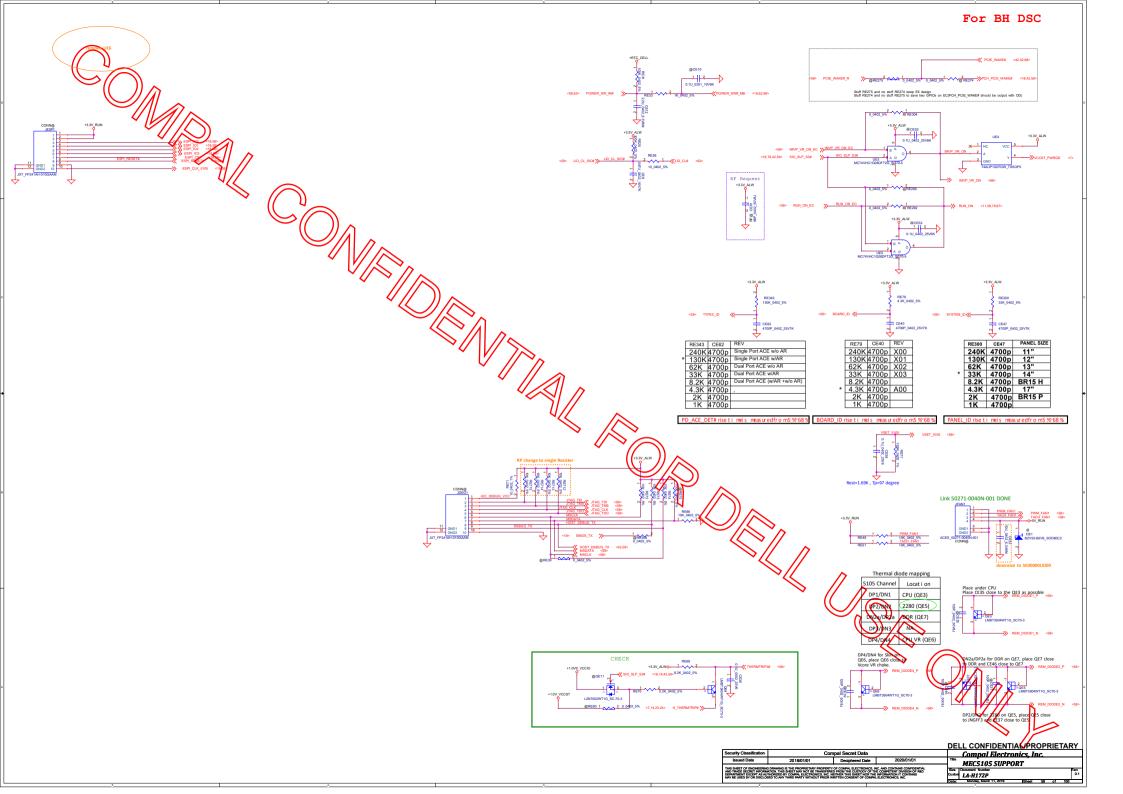




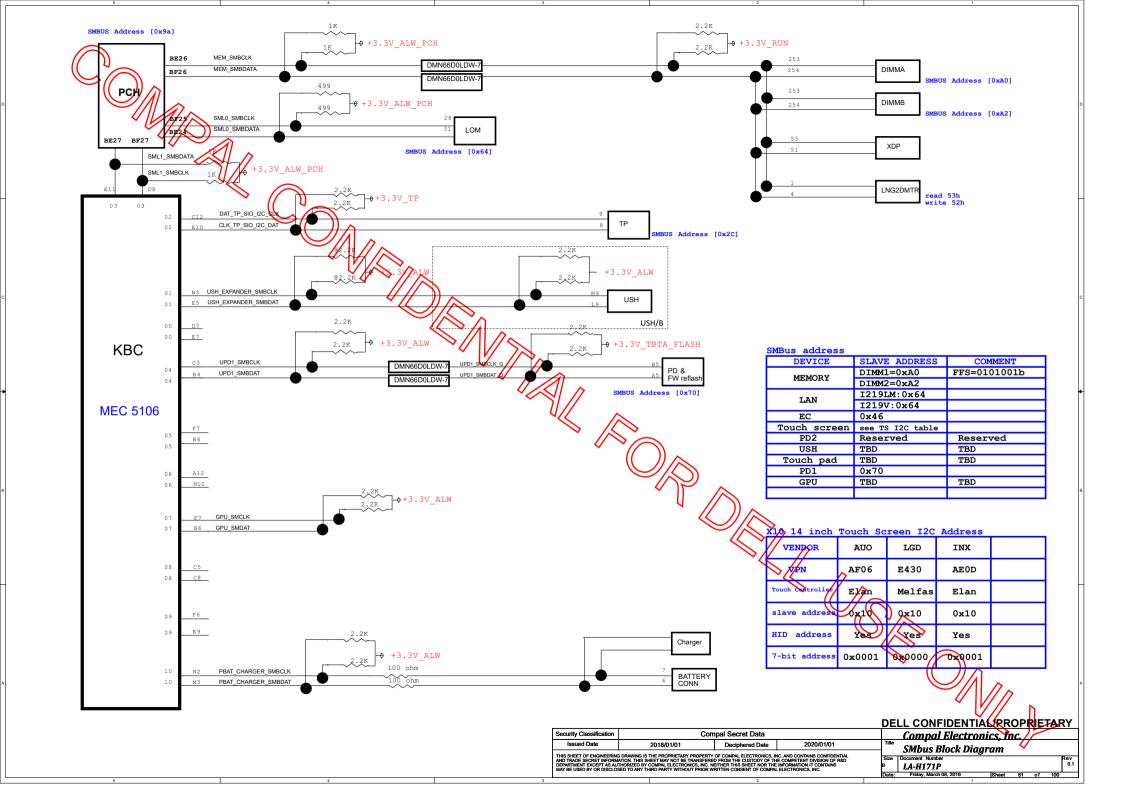


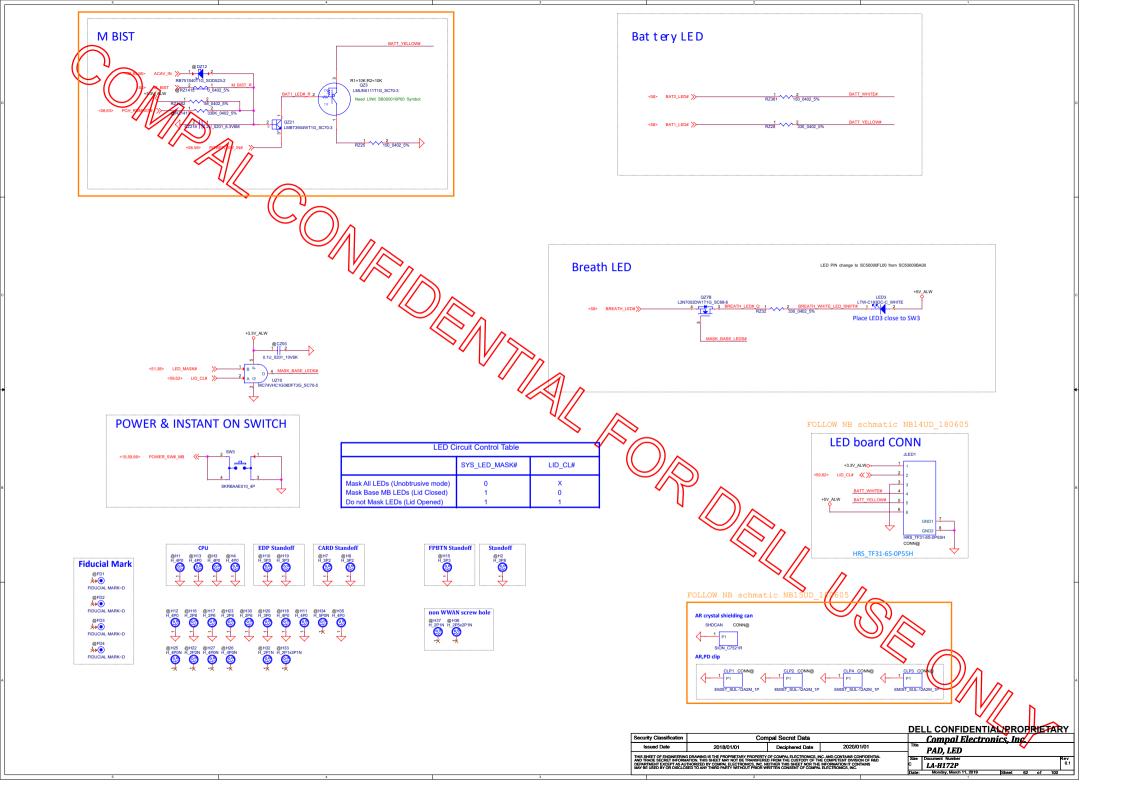


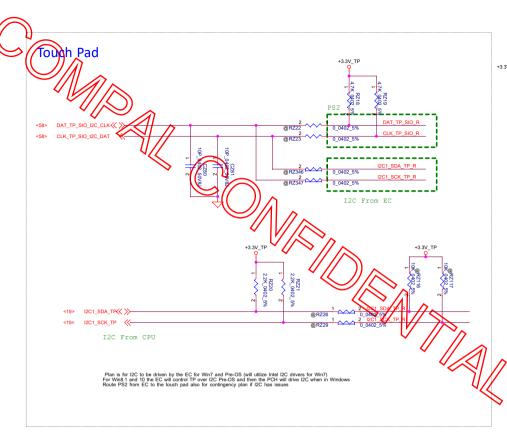


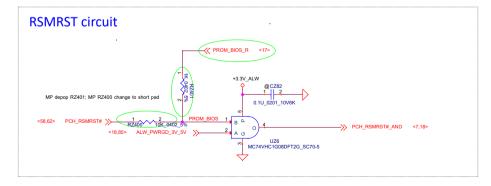


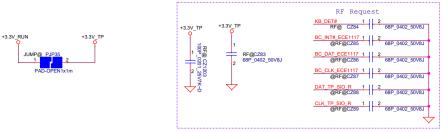




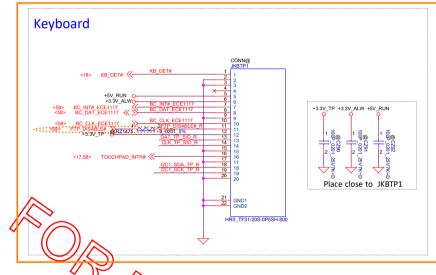








JKBTP1 FOLLOW NB schmatic NB15UD 180628

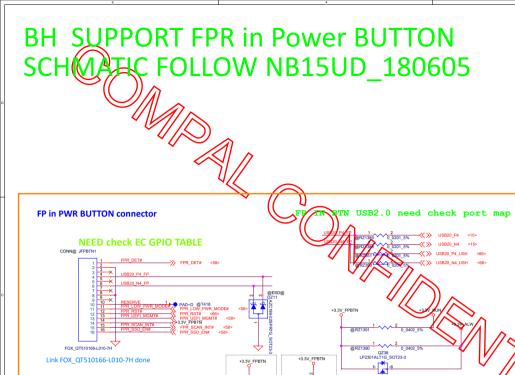


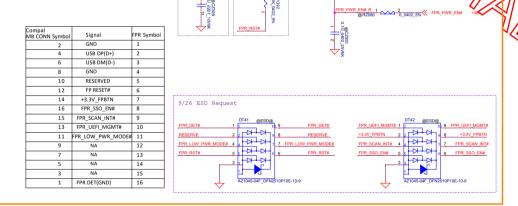
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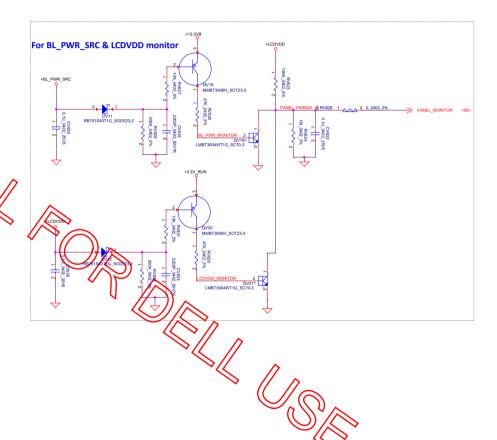
Issued Date 2018/01/01 Deciphered Date 2020/01/01

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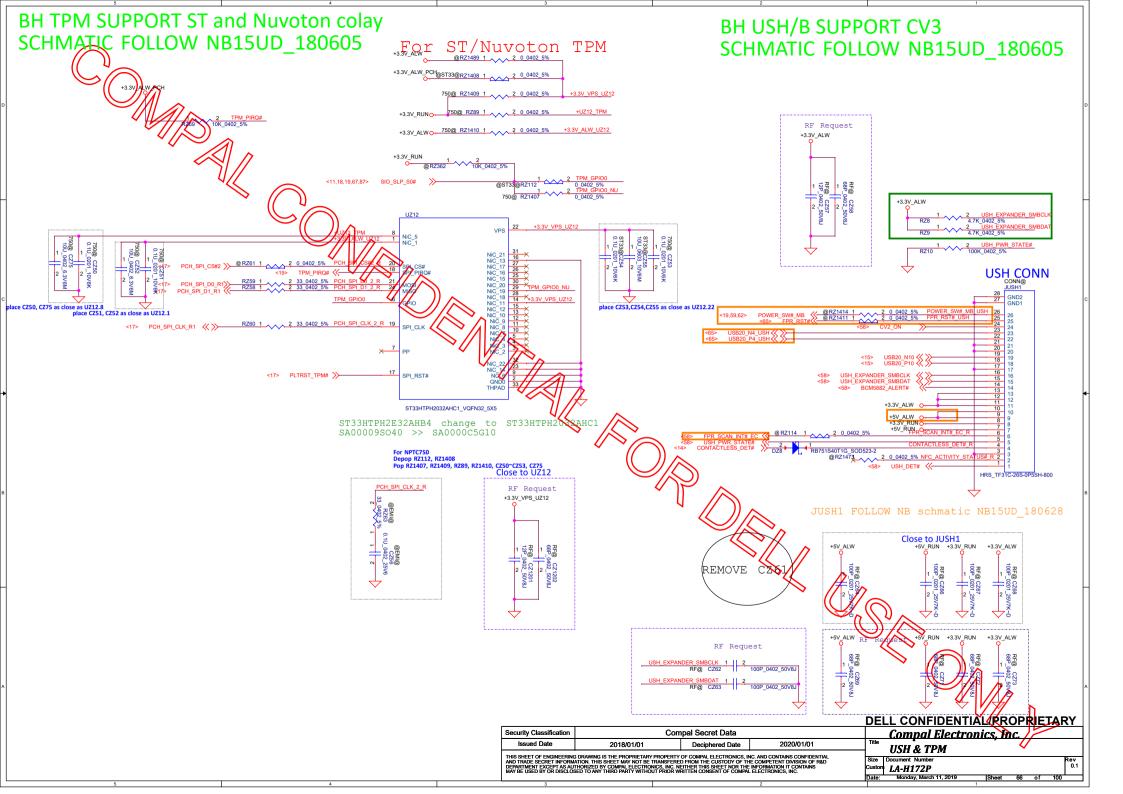
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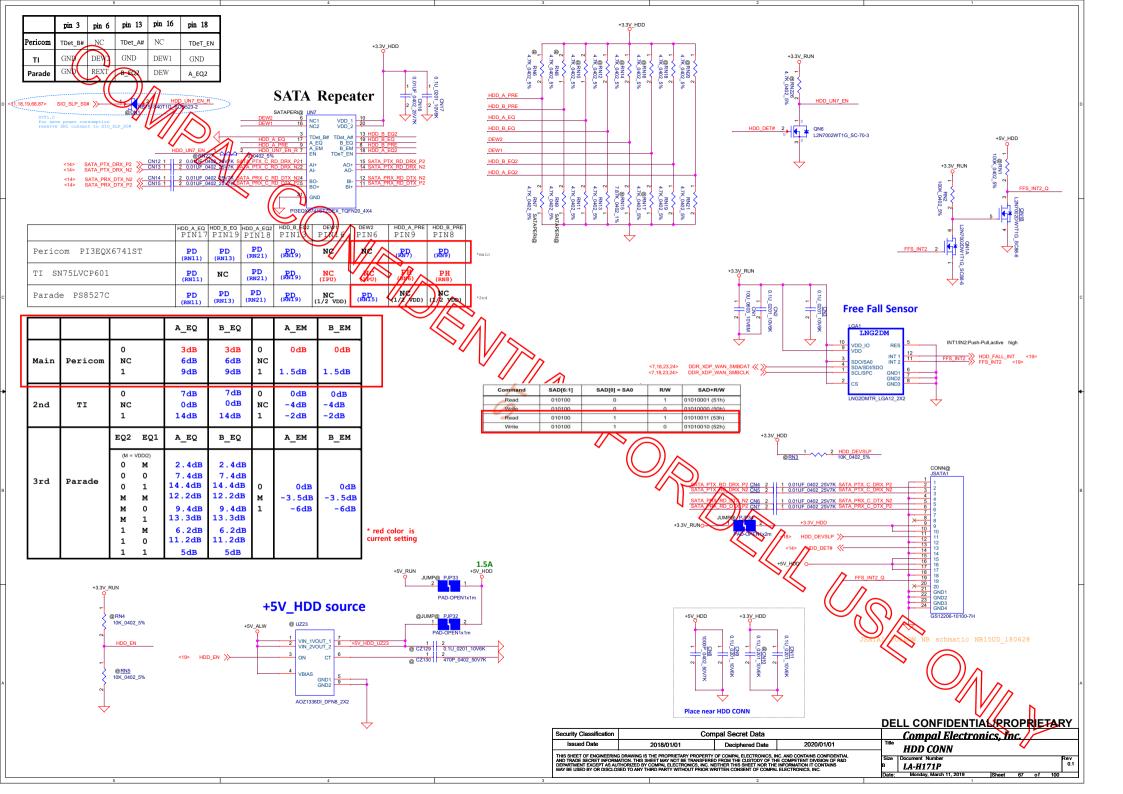
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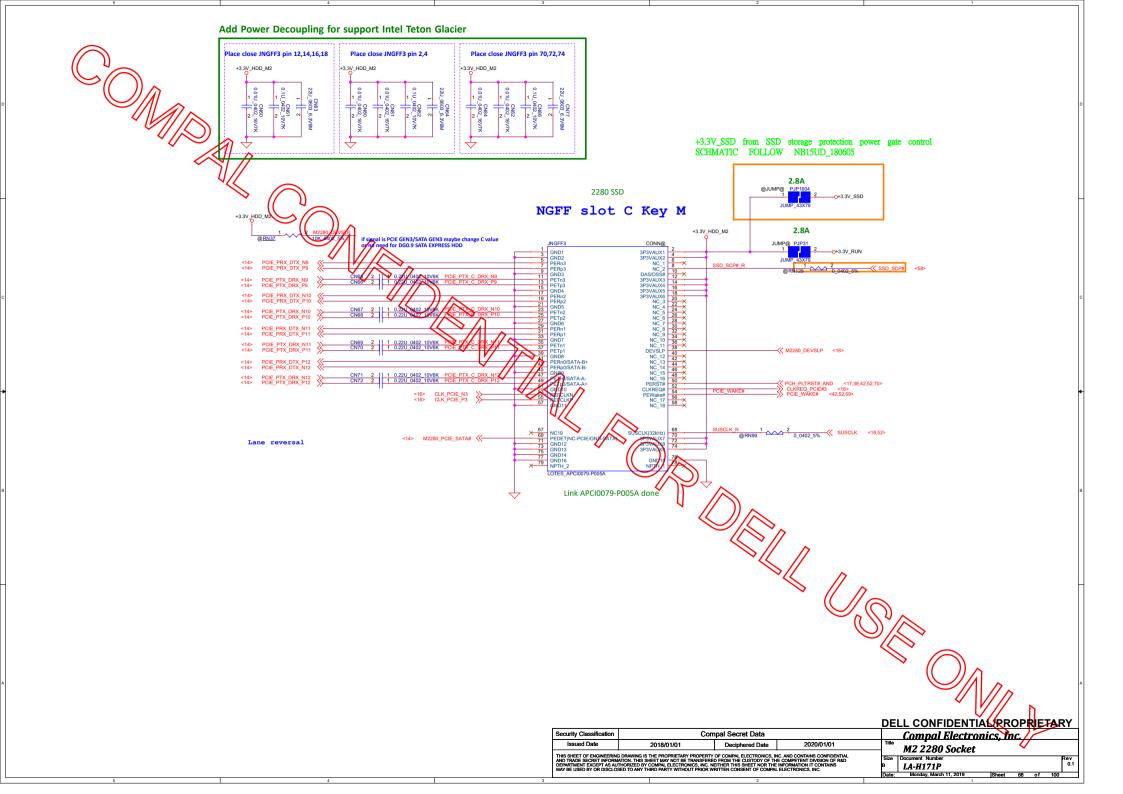
Compal Electronics proc.

Title
FP in PWRBTN

Step
Decument Number
LA-H172P
Date: Monday, March 11, 2019
Bissel 65 of 105

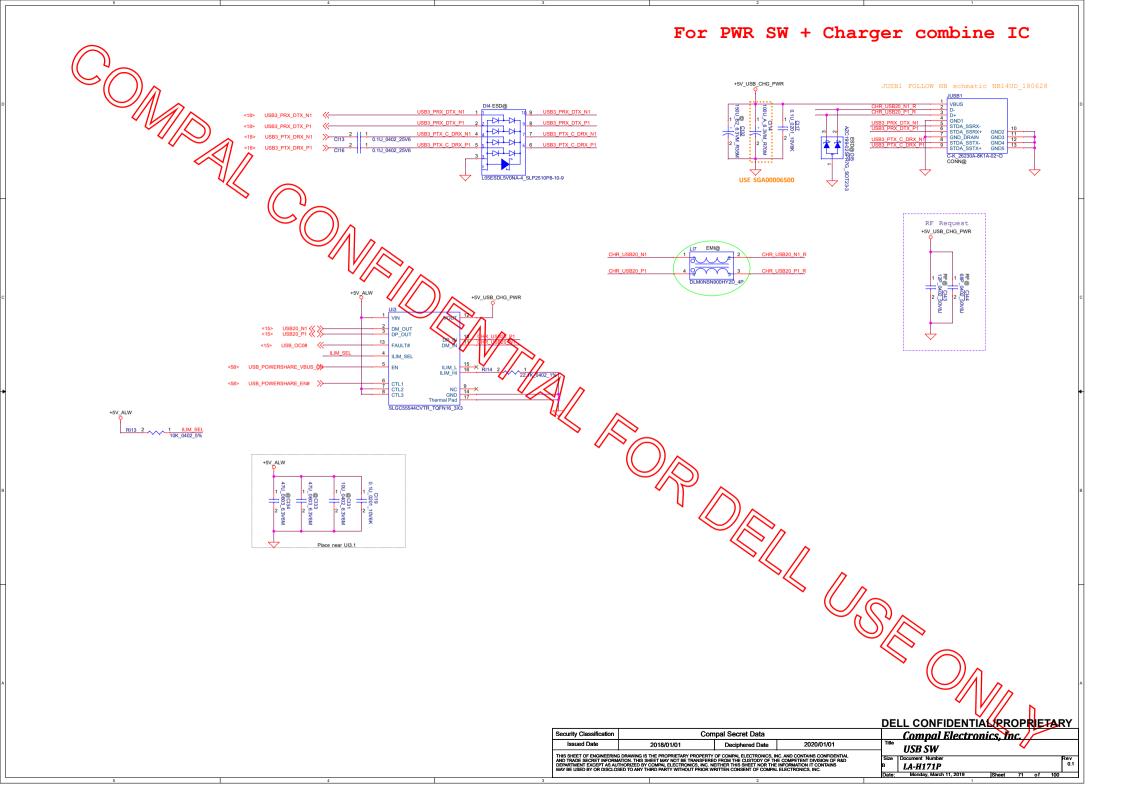


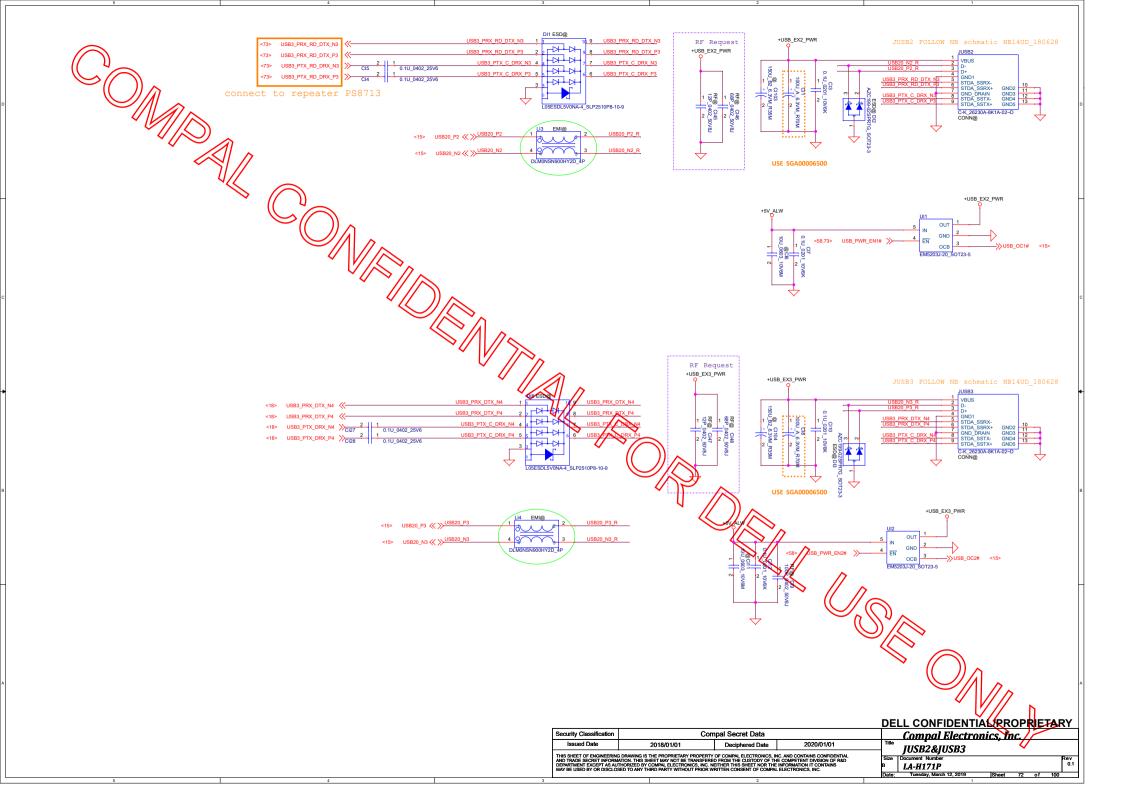


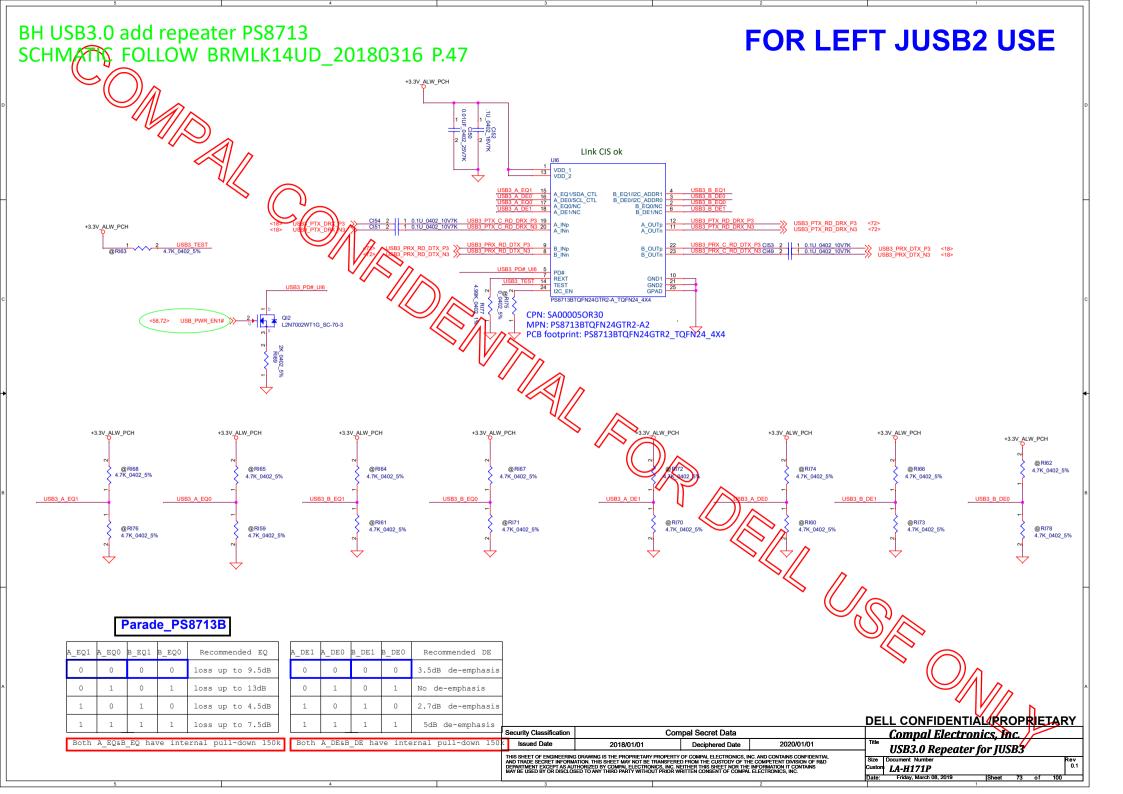




For PCIE Interface support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3 AUX) 1 2 DR22 1 1U_0201_10V6M RF Request +3.3V_MMI_IN +3.3V_MMI_AUX EMI depop locat i on JSD1 FOLLOW NB schmatic NB14UD_180628 change to micro SD <14> HOST_SD_WP# >> +3.3V_RUN_CARD +1.8V_RUN_CA DELL CONFIDENTIAL PROPRIETARY Compal Electronics, Ing. Security Classification Compal Secret Data 2018/01/01 Deciphered Date Card Reader LA-H171P Monday, March 11, 2019



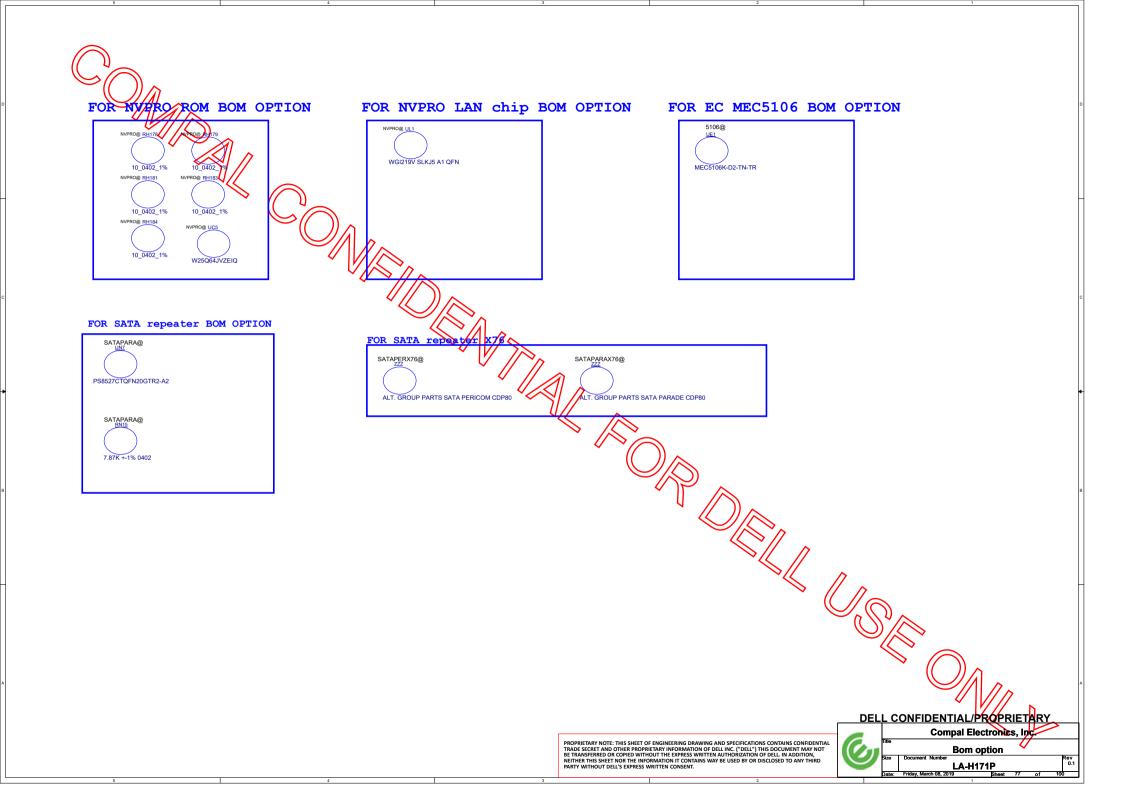


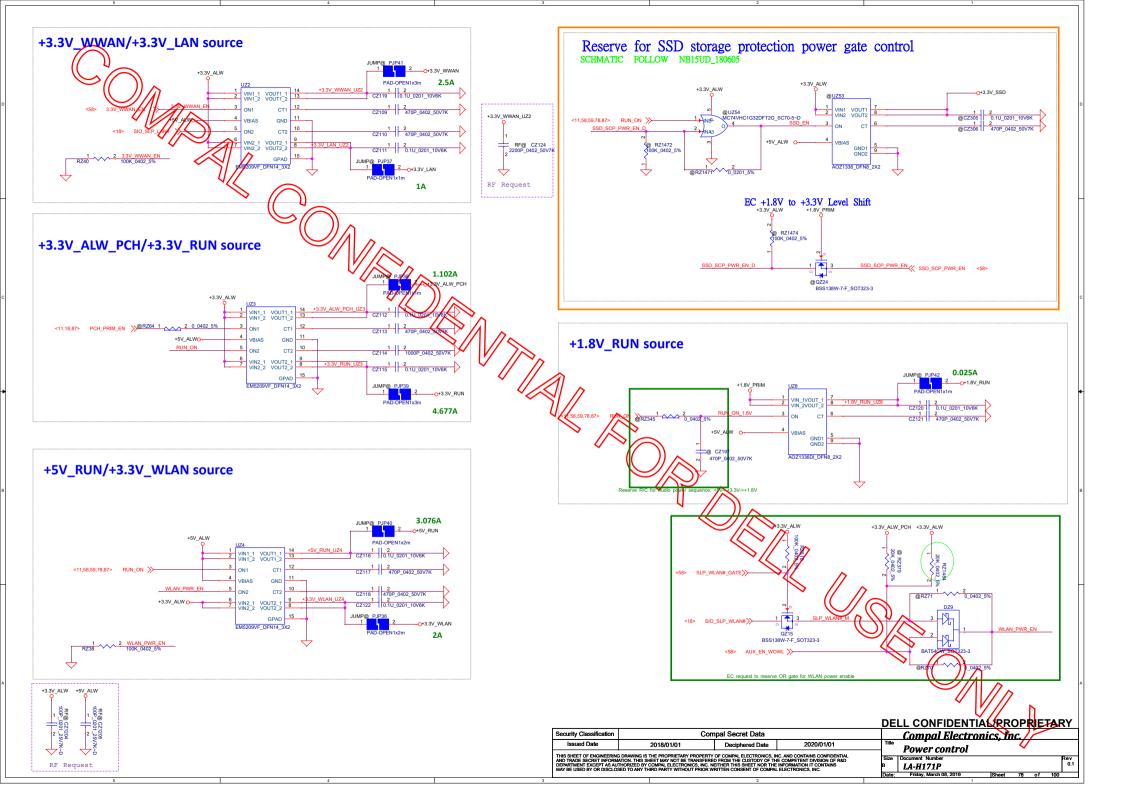








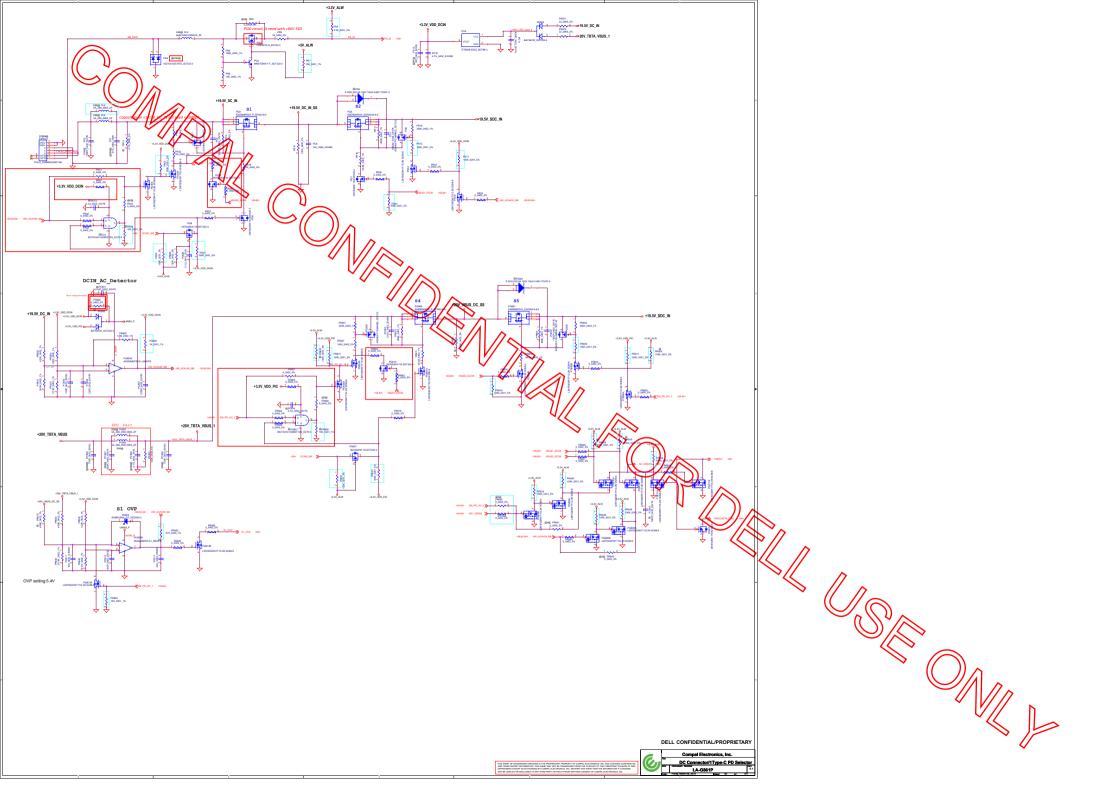


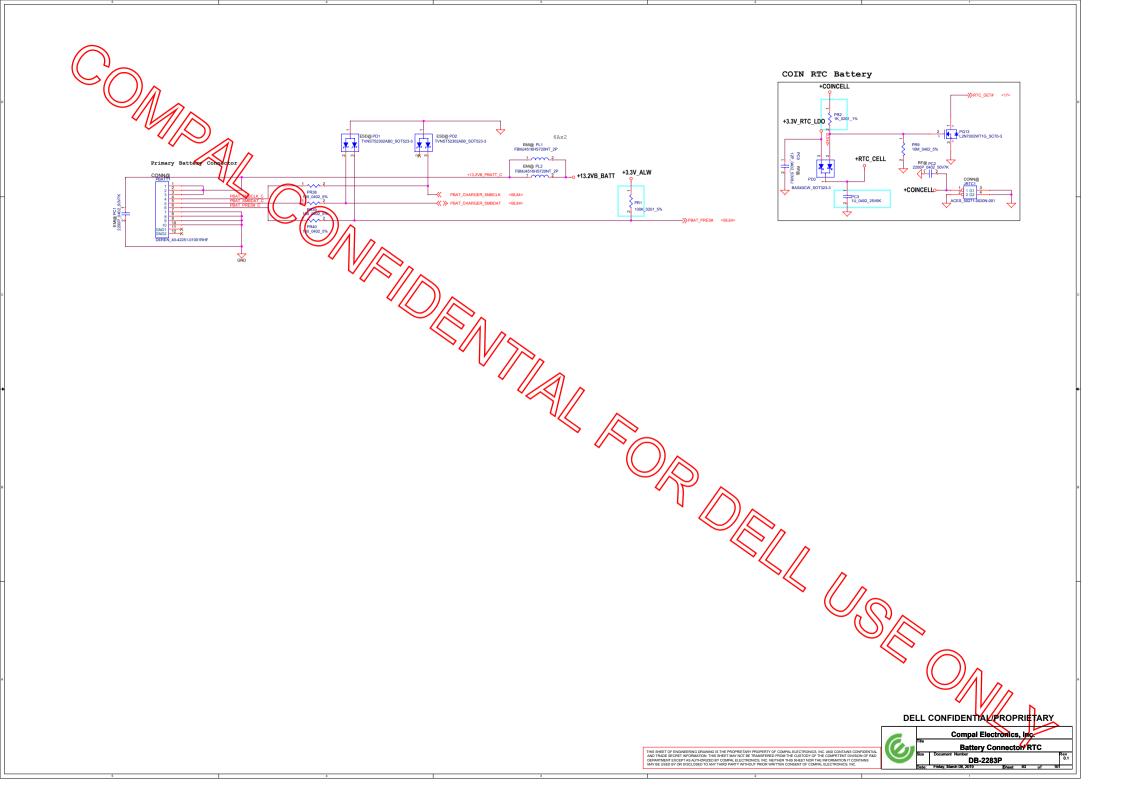


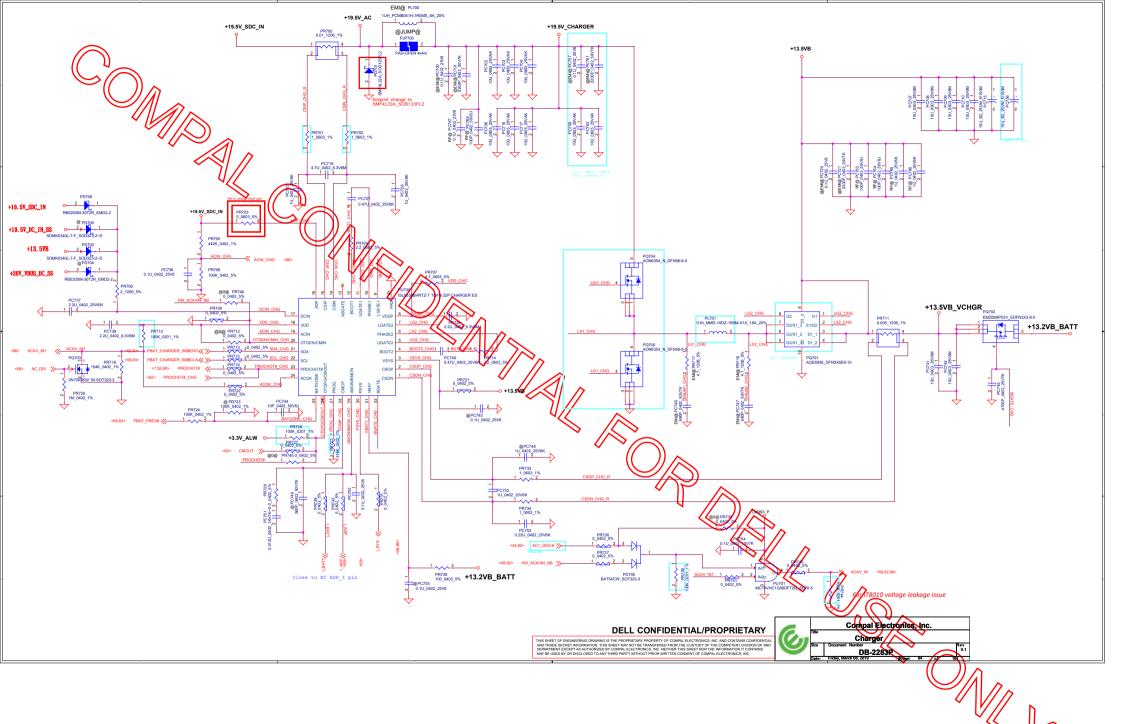


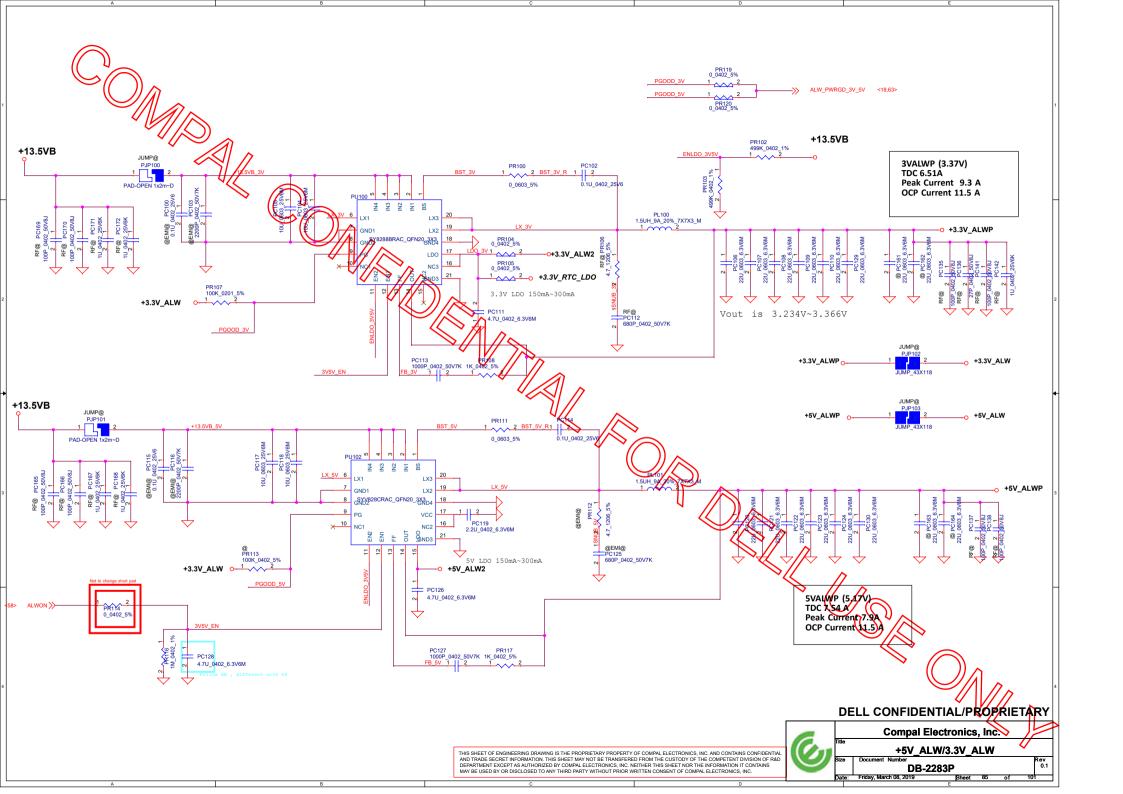


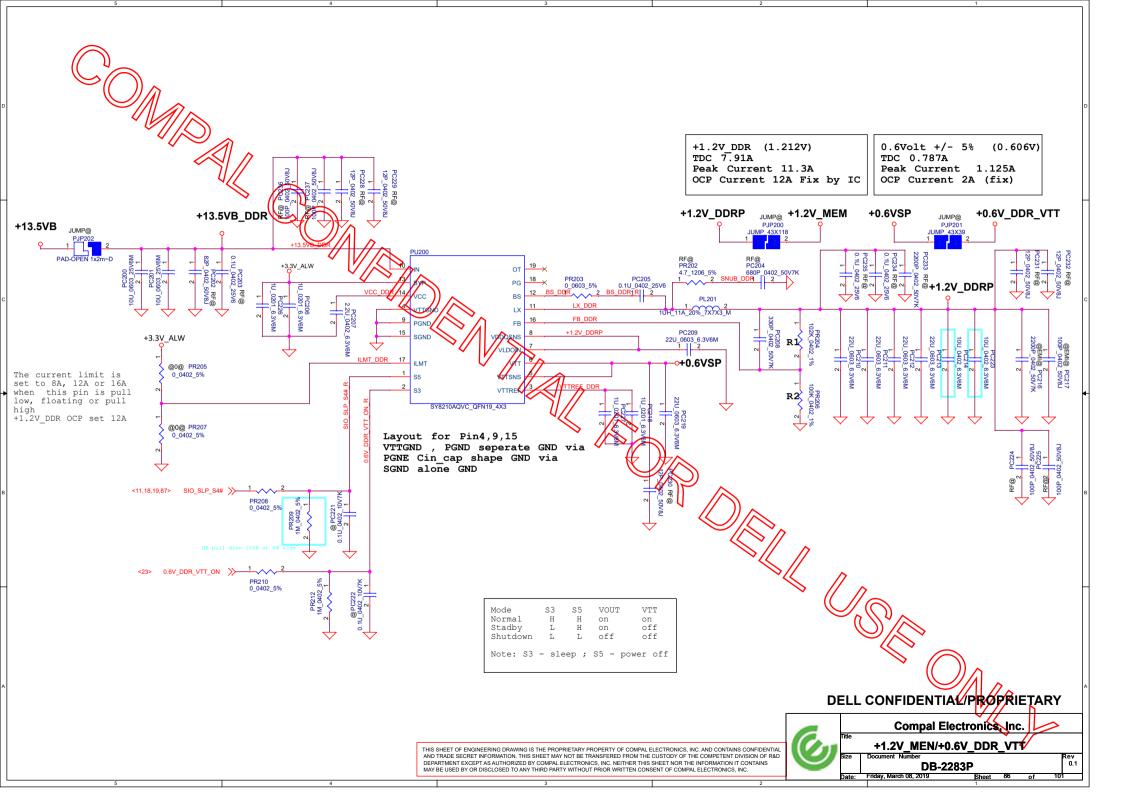


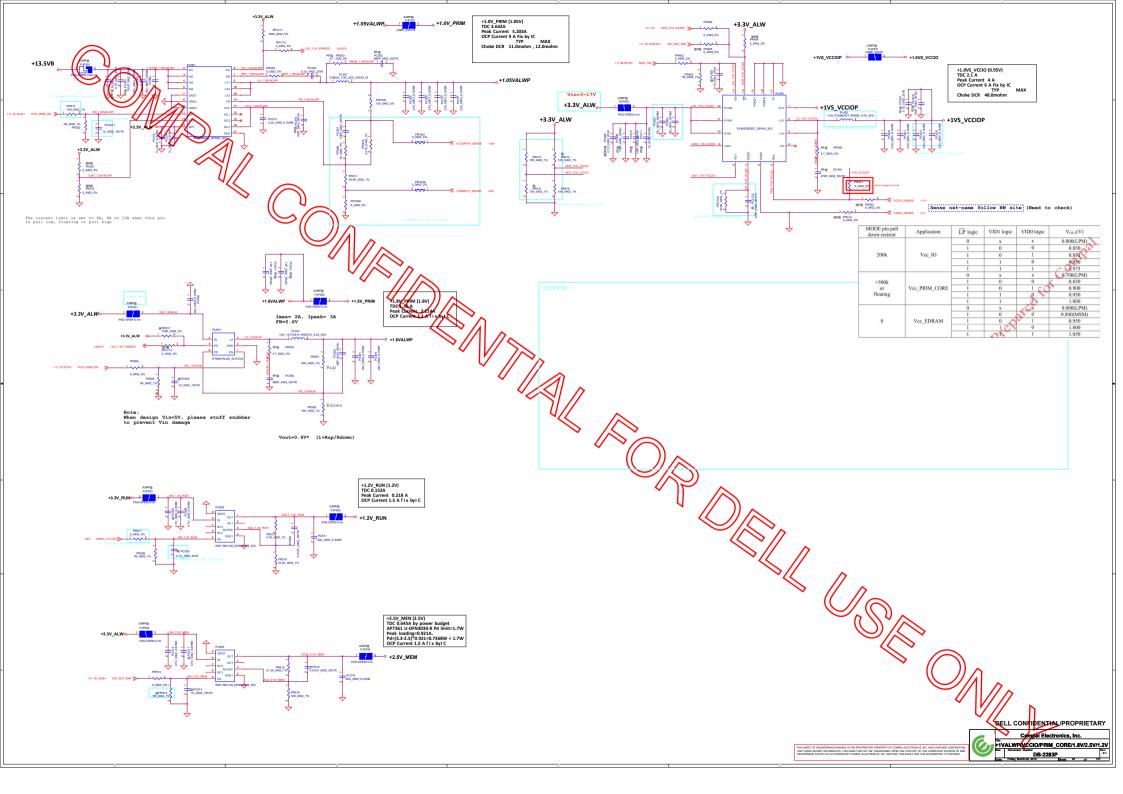


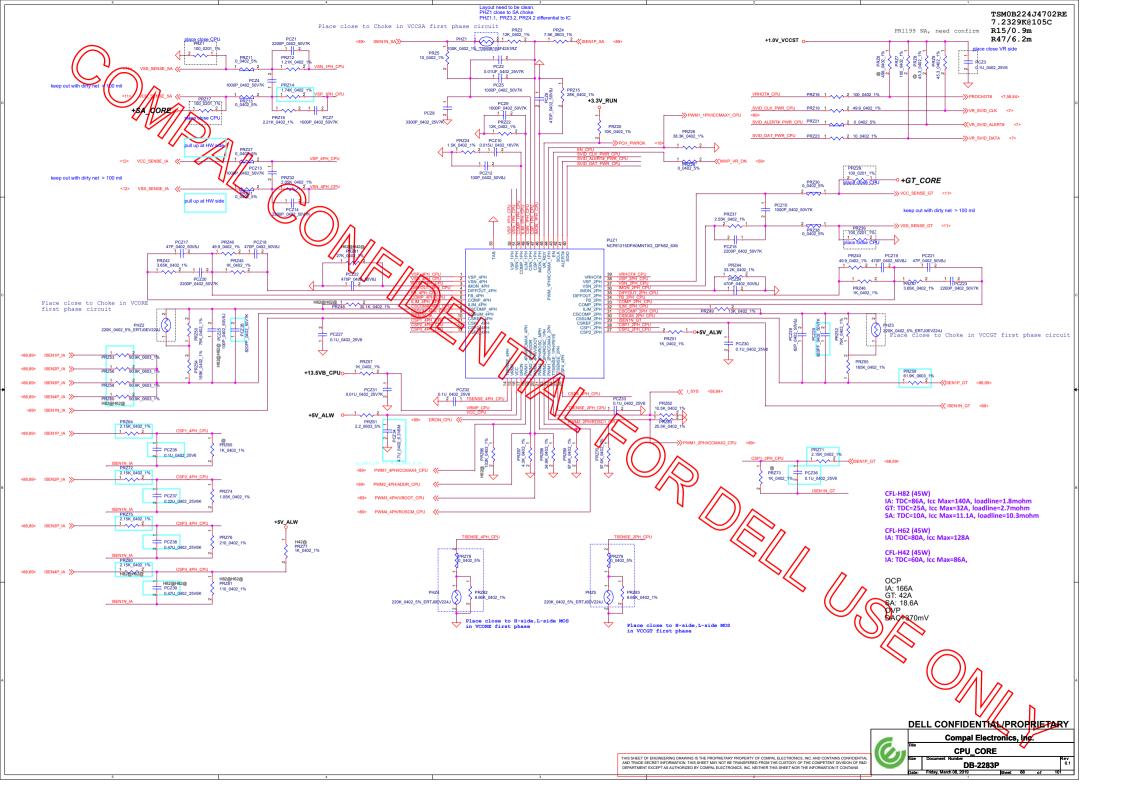


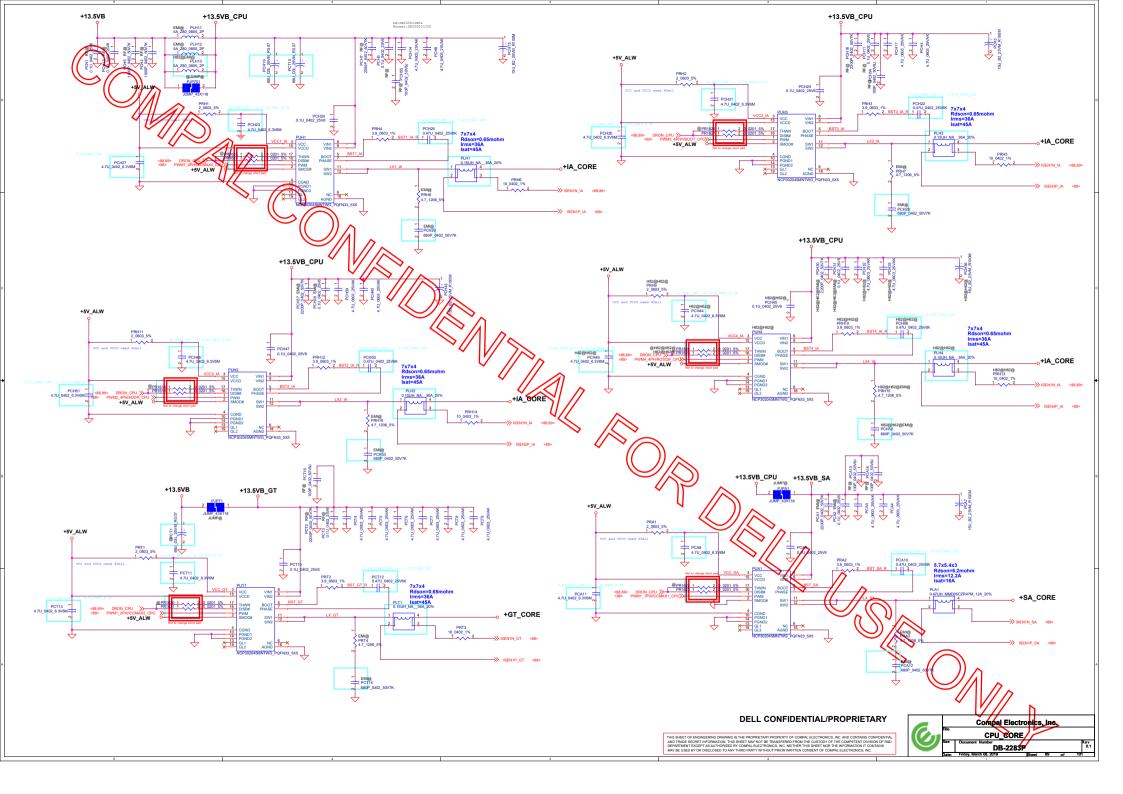


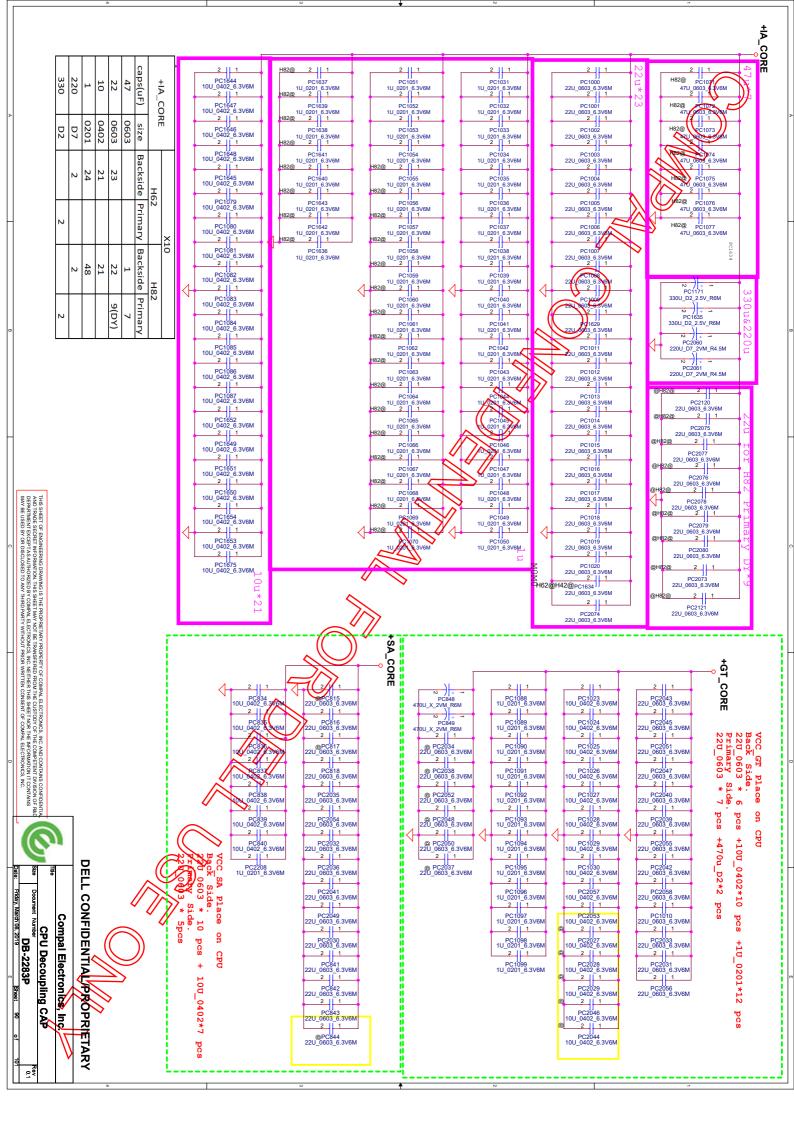


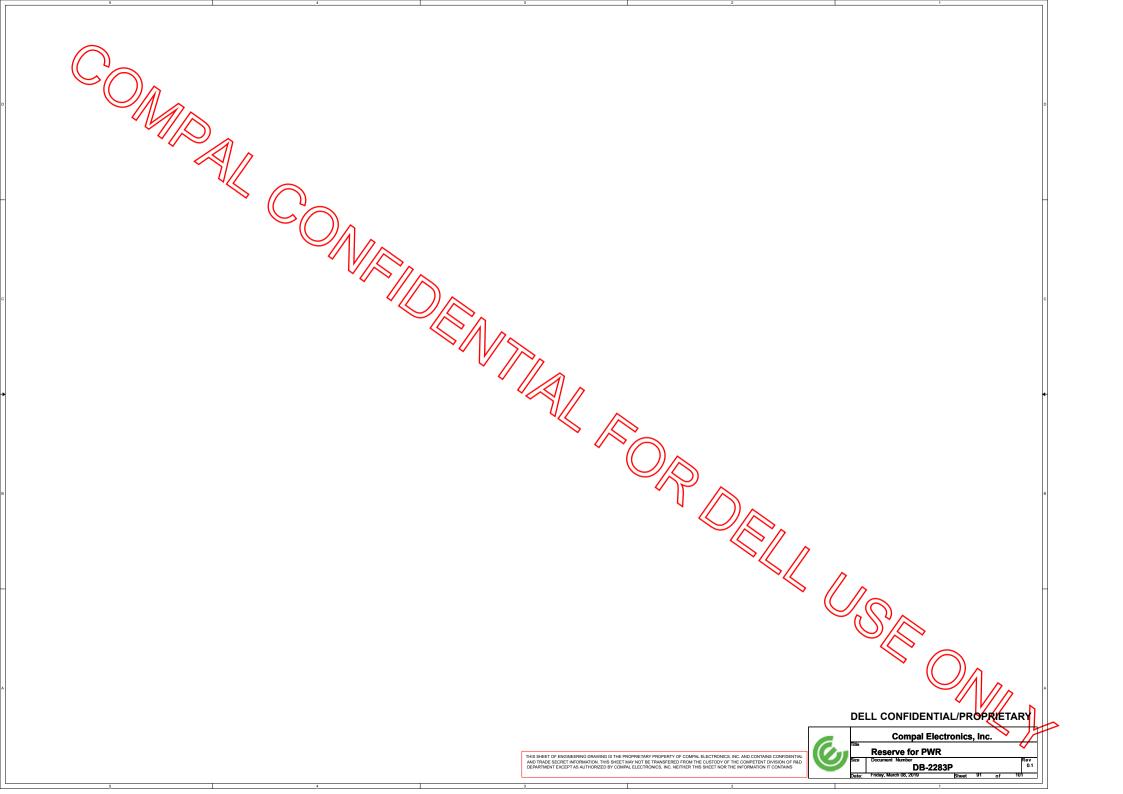


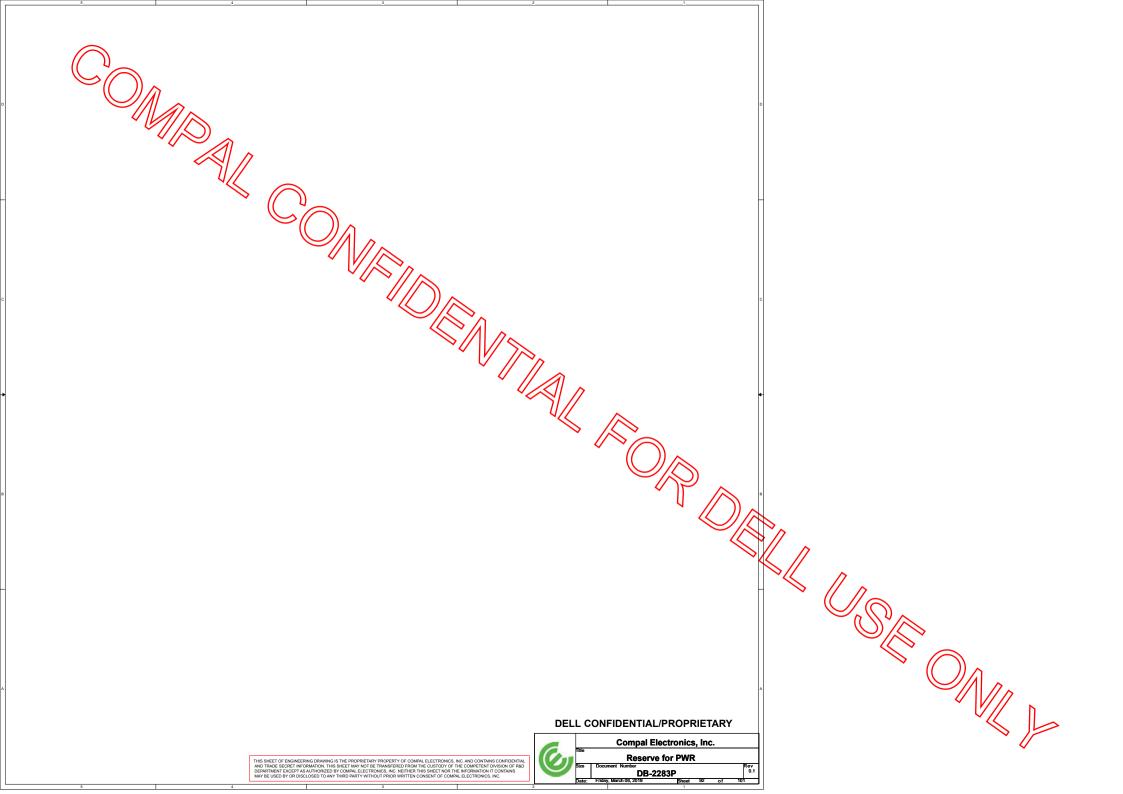


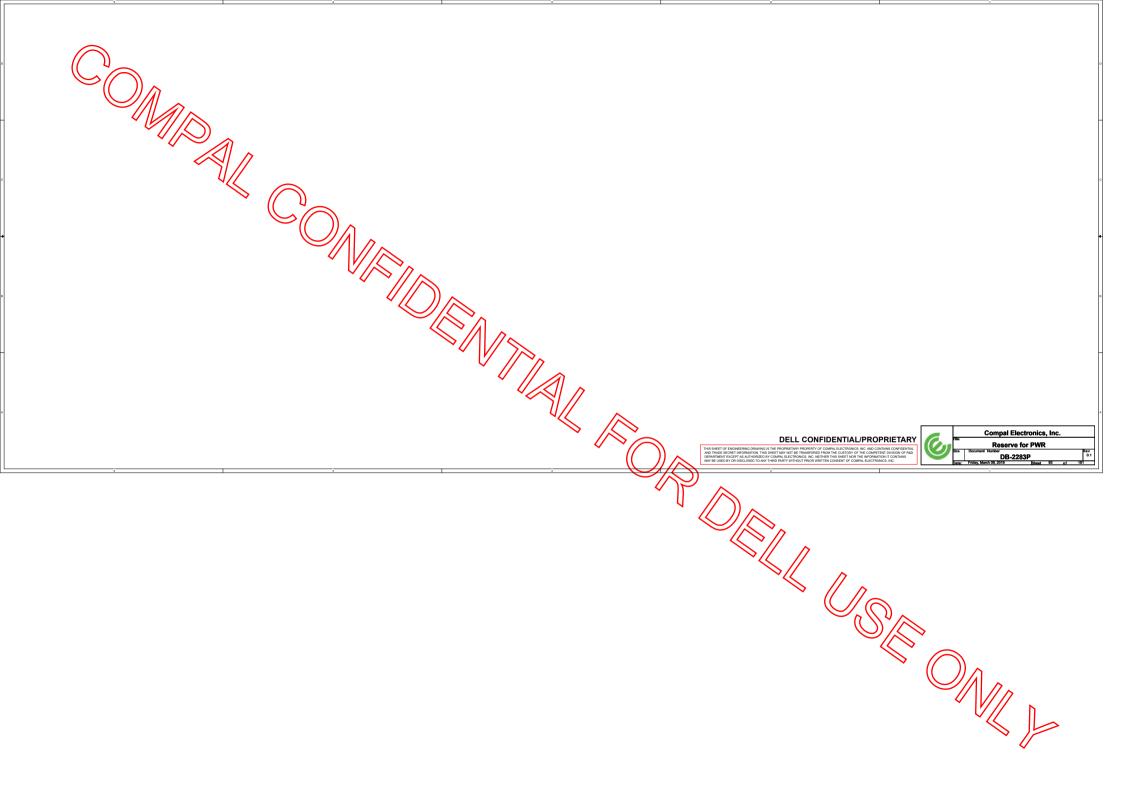


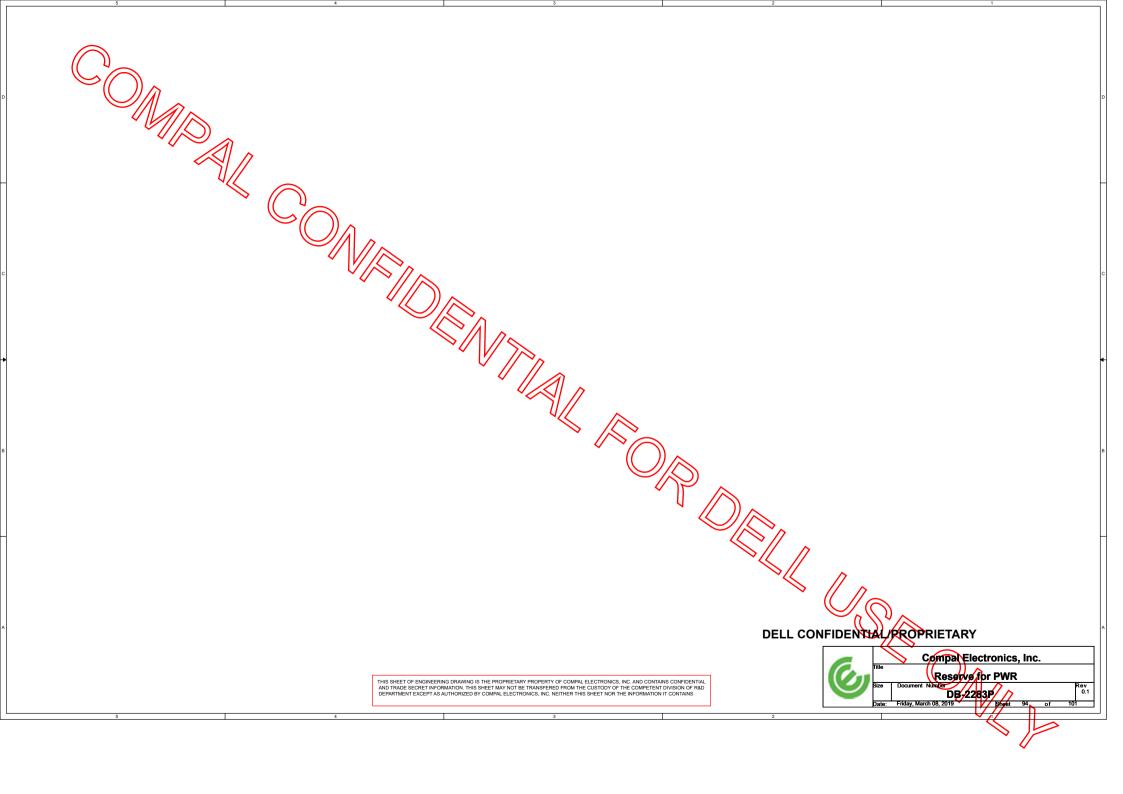


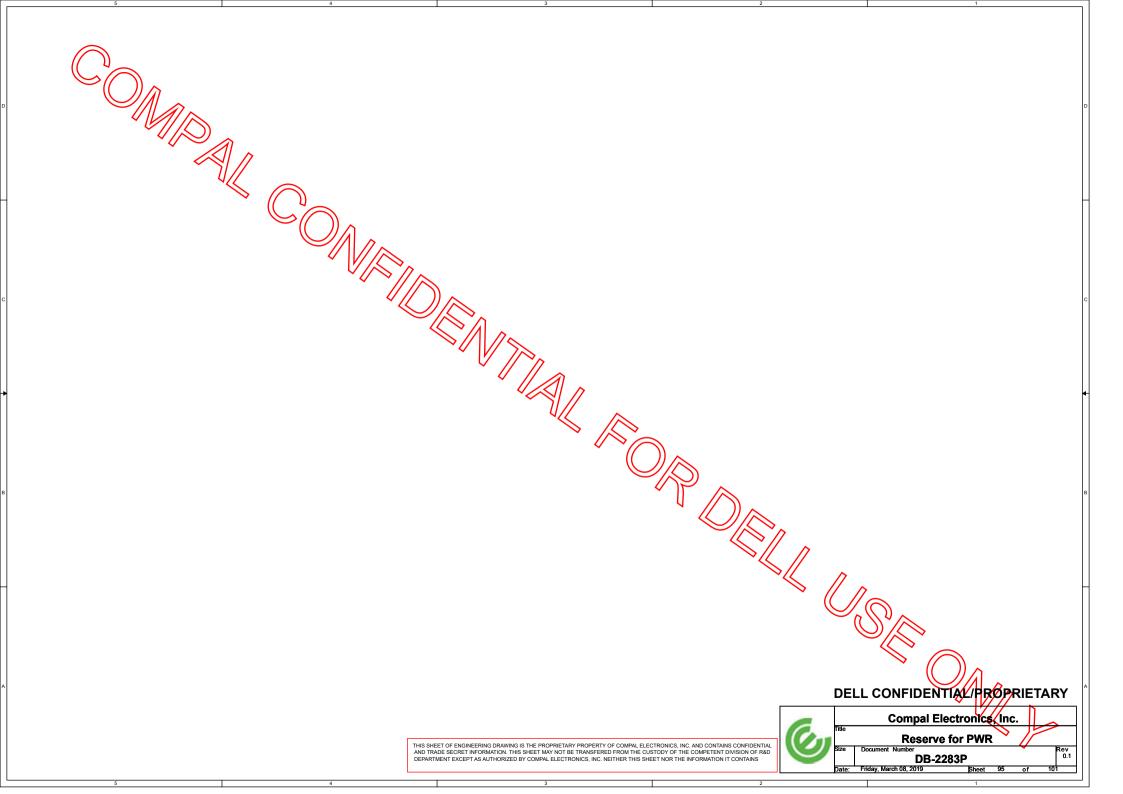


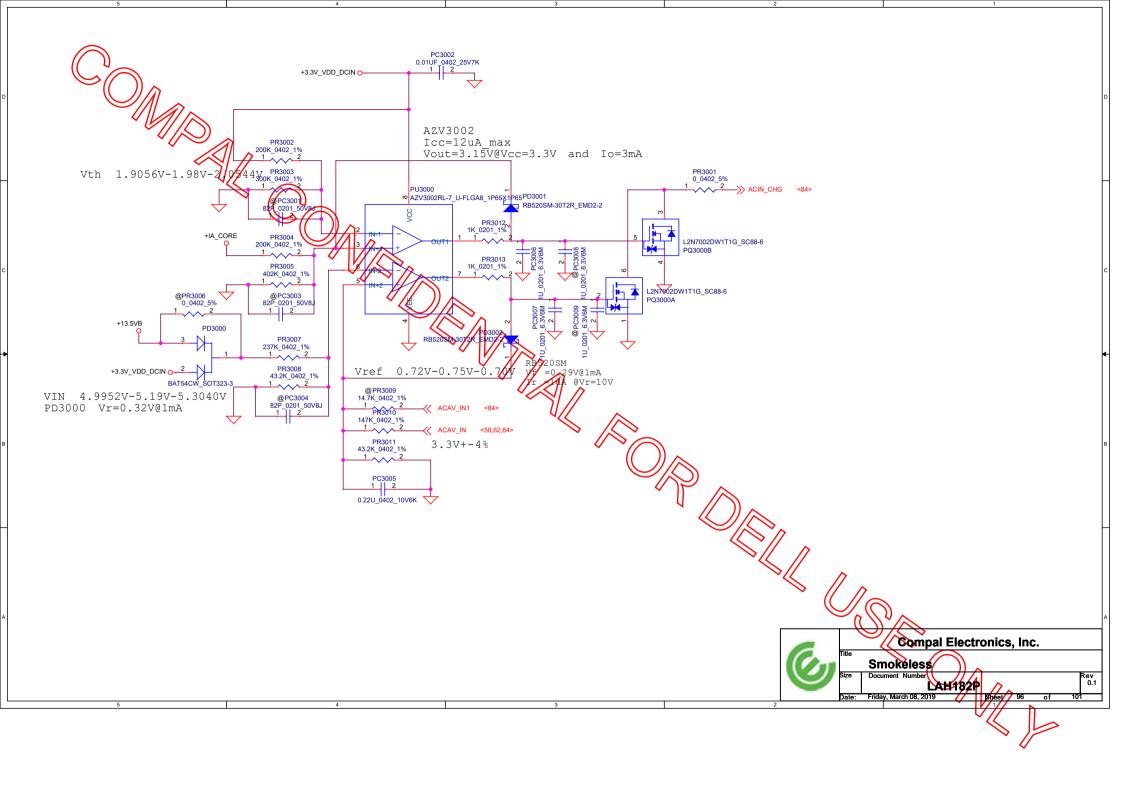


















Item P		Solution Description Description	Rev.
item	Title	Description Description	Remark
1	change 0 Ohm to Short pad:	UMA(55): PR19,PR20,PR22,PR25,PR861,PR42,PR44,PR46,PR47,PR49,PR104,PR105,PR119,PR120,PR709,PR713,PR715,PR719,PR721,PR722,PR727,PR729,PR731,PR736,PR737,PR740,PR741,PR743,PR814,PR816,PR818,PR820,PR826,PR827,PR829,PR1652,PR836,PR840,PR844,PR853,PR854,PR858,PR859,PRZ11,PRZ13,PRZ27,PRZ31,PRZ78,PRZ79,PRZ30,PRZ38,PRZ21,PRZ28,PR1651,PR1649 DIS(4): PR1302,PR1305,PR1315,PR1406	1
		add note: Not to change short pad PR866,PR114 PR1616,PR1618,PR1620,PR1626,PR1624,PR1622, PR1617,PR1619,PR1621,PR1627,PR1625,PR1623	
2	Power path S1 fast turn off circuit simplify	un stuff PC13,PU3,PR45,PC814,PU801,PR855	Follow NB
3	+3.3V_VDD_DCIN LDO circuit	change PR871 and PR872 to 22_0805_5% (SD002220A80) Function field 39.10 PD803 Pin 1 add net name: +20V_LDO_input **Please check layout trace at least 20 mil Delete PR868 colay footprint	Follow NB
	Character and CDIT OND 1:4	PR3010 change value from 14.7K to 147K(SD034147380) PR3011 change value from 4.32K to 43.2K(SD034432280)	Follow NB,for more sequence margin.
4	Charger UVP and CPU OVP circuit modify	Change PU3000 from SA0000A6500 to SA0000A6400	SA0000A6500 test has abnormal problem when default initial
5	Common BOM modify	Change PLH1,PLH2,PLH3,PLH4,PLT1,PL1302,PL1301 from SH00001D800 to SH00001EE00	change to common PN
6	Dr.mos Main/2nd/3rd source is group alternative, need to place on same layer for SMT process.	Change PR1616,PR1618,PR1620,PR1626,PR1624,PR1622 from 0_0402 to 0_0201 Change PR1617,PR1619,PR1621,PR1627,PR1625,PR1623 from 0_0402 to 0 0201	Placement need modify the x76 components on the same layer
7	Fine tune GPU enable sequence	Change PR1309 from 100K_0402_1% to 1K_0402_1% (SD034100180)	EE requirements Fine turn GPU Power sequence
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Ver.	Version Change List (P. I. R. List) Issue Solution					
Item	Page	# Date	Description	Description	Rev.	
1	70	2019/05/23	follow BH ARD(v0.5) define	JSD1 connector use Micro SD type,QR1.3 change to gnd	0.1(X00)	
2	44	2018/05/23	PD USB2.0 source from PCH follow X10 NB	PD USB2.0 source change from TBT to PCH depop RT402,403 pop RT400,RT401	0.1(X00)	
3	46	2018/06/05	add TBT type c short protection circuit	implement AR type c short protection circuit ,add RT190~RT197,CT326~CT329,CT95~CT98,RT488~RT491,RT219~RT222	0.1(X00)	
4	43	2018/06/05	change PD and AR power rail	1.PJP6 no solder,RT48 pop 2.add RT399 pop,RT398 depop for +3.3V_VDD_PIC option 3.add RT482 depop,RT483 pop for +3.3V_VDD_PIC_PDA option,remove PJP7	0.1(X00)	
5	38	2018/06/05	follow NB JEDP1, JTS1 pin define	remove LV27,DV4,JIR1,UH1.M6,UH1.N8 add JIRTS1,pin define follow NB add RV733,RV732 JEDP1.1 +5V TSP- +TS PWR SRC JEDP1.2 USB20 N9 R- NC JEDP1.3 USB20_P9_R- NC QV8.1 +5V TSP- +TS PWR SRC check TS_INT#,TS_IZC_SDA,TS_I2C_SCL GPIO	0.1(x00)	
6	11	2018/06/08	power follow compal naming rule, HW synchronize change net name	VSS IO_SENSE - VSSIO_SENSE VCC IO_SENSE - VCCIO_SENSE VSS_GT_SENSE - VCC_SENSE_GT VCC_GT_SENSE - VCC_SENSE_GT VCO_SA_SENSE - VCC_SENSE_SA VSS_SA_SENSE - VSS_SENSE_SA VCC_SENSE - VCC_SENSE_IA VSS_SENSE - VCC_SENSE_IA VSS_SENSE - VSS_SENSE_IA +FWR_SEC_+13.5VB +TBTA_VOGS_1 - +20V_TBTA_Vbus_1	0.1(X00)	
7	56	2018/06/08	change audio codec solution to ALC 3204	follow ARD implement ALC 3204 schmatic(UA1)	0.1(X00)	
8	66	2018/06/08	follow USH/B pin define	JUSH1 pin define follow NB, support USH/B CV3 remove LZ2,CZ61 add RZ1414 RZ114 pop 1. JUSH.1 +PWR SRC R→ POWER SW#_MB USH 2. JUSH.2 NC→ FPR RST#_USH USH 3. JUSH.4 POA WAKE#_R→ USB20 N4 USH 4. JUSH.5 EC FPM EN→ USB20 P4 USH 5. JUSH.17 NC→ +5∨ ALW 6. JUSH.21 USH RST#_R→ FPR SCAN INT#_R 7. JUSH.25 GND→ NFC ACTIVITY STATUS#_R	0.1(X00)	
9	68	2018/06/08	Reserve for SSD storage protection power gate control schematic	1.add PJP1604,RN131 RZ110 for +3.3V_SSD power option 2.add RN129 for SSD protection 3.add UZ53,UZ54,RZ1471,RZ1472,CZ305,CZ306,RZ1474,QZ24/(depop) 4.check SSD_SCP#,SSD_SCP_PWR_EN GPIO	0.1(X00)	
10	62	2018/06/08	add M-BIST HW Circuit	1.remove HDD LED MUX circuit(remove QZ2,RZ25) 2.add M_BIST circuit(DZ12,RZ1415,RZ1482,RZ1413,CZ218,QZ21,QZ3,FZ25)	0.1(X00)	
11	17	2018/06/08	BOM option for VPRO, non-VPRO	1.UC6 change to SA00005VV20(follow NB) 2.NVPRO@ RH352,RH353,UC6,CH270,RH177,RH657,RH658,RH659,RH660,UC5,RH178,RH179,RH181,RH183,RH184 3.VPRO@ UC5,RH178,RH179,RH181,RH183,RH184,UL1 4.add NVPRO LAN CHIP UL1 SA00009340L 5.RZ59,RZ58,RZ60 change to 33 ohm and BOM structure NA DELL CONFIDENTIAL PROPE Compal Electronics, In		
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12	18	2019/06/08	glitch schmatic	SIO_SLP_SO# add RH640 100k PU(depop) to +3.3V_ALW_PCH	0.1(X00)
13	62	2018/06/08/	follow NB AR use clip type shielding can	SHDCAN footprint change to SION C7521R 1P-T add 4 clip for AR,PD location:CTP1,CLP2,CLP3,CLP4	0.1(X00)
14	16	2018/06/08	change crystal size, follow NB	YH2 SJ10000VK00→ SJ10000XF00 YV1 SJ10000EQ00→ SJ10000ZL00	0.1(X00)
15	51	2018/06/08	RJ45 21FDs	remove UL2,QL1 add RL20 UL1.27 LOM_SPD100LED_ORG#→ LOM_CONNLED_GRN# UL1.25 change to TP(LOM_LED2) QL1.4 LOM_SPD100LED_ORG#→ LOM_CONNLED_GRN# QL1.3 LED_100 ORG#→ LED_GRN# JLOM1 follow NB_180615	0.1(X00)
16	58	2018/06/19	naming change	UE1.K4 DCIN1_EN→ DCIN2_EN UE1.L12 DCIN2_EN→ DCIN1_EN UE1.M6 VBUS1_ECOK→ VBUS2_ECOK UE1.N3 VBUS2_ECOK→ VBUS1_ECOK UE1.L7 1.8V_1.0V_PWRGD→ PRIM_PWRGD(add RE361)	0.1(X00)
17	63	2018/06/19	add programming circuit	JSPI1.17 add net PROM_BIOS_R add RZ401,RZ400 to PCH_RSMRST# RH185 deopo	0.1(X00)
19	73	2018/06/26	USB3.0 length over spec,add repeater	add UI6 USB3 repeater and related components	0.1(X00)
20	17	2018/06/28	Reserve for Panel side TS PH voltage problem $rac{4}{3}$ schematic	/ add RH566 pop 2 add CH8/RH104 depop 3.JEDP1.5 TOUCH_SCREEN_PD# TOUCH_SCREEN_PD#_R	0.1(X00)
21	63	2018/06/28	X10 KB support KB disabel function	1.add RE1475 pop 2.JKBTP1.10 against TP DISABLE#_R 3.TP_DISABLE#_add_pot_to_EC	0.1(X00)
22	21	2018/06/28	follow CFL H PDG 1P8 page.623	1.+1.0V_XTAL add 2x 22nF 0603 (add CH349 depop) 2.+1.0V_AMPHYPLL add 2x 22nF 0603 (add CH350 depop) 3.CH32 change to 1x4.7vF 0402	0.1(X00)
23	21	2018/07/03	follow CFL H PDG 1P8 page.623	1.+1.0V_XTAL Series Inductor 0603 2)2 Uh depop(LH421) 2.+1.0V_AMPHYPLL Series Inductor 0603/2 2 Uh depop(LH423)	0.1(X00)
24	12	2018/07/03	+1.0V_VCCSFR add LPF	add LC562depop,RC422 pop	0.1(X00)
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25	58	2918/07/12	GPIO modify	remove RE566,RH639,RH638,RH624,RH360,RH330,RH621,RH622,RH623,RE101,RH207,RH322,RH425 add RE340,RH661 1.UE1.D1 HDD EN EC → TBT RESET_N_EC 2.UE1.D6 EC_FPM_EN → FREE 3.UE1.E4 POĀ WAĶE# → FREE(VCI_IN3#) 4.UE1.J6 CG6_ACPI_CHECK → NB_MODE# 5.UE1.K1 PCH PLITST# EC → WWÄN GPIO CTRL 6.UE1.L8 TBT_RESET_N_EC → FPR_SCAN_INT# 7.UH1.AP21 RTD3 CIO PWR EN → FREE 8.UH1.AE43 NC → RTD3 CIO PWR EN 9.UH1.AR32 TBT RTD3 WAĶE# → NC 10.UH1.T47 NC → TBT RTD3 WAĶE# 11.UH1.BE20 LPSS UART2_TXD → FREE 12.UH1.AW21 CNV ĒN# → FREE 13.UH1.BE23 PCH_TBT PERST# → FREE 14.UH1.BE33 PCH_TBT PERST# → FREE 14.UH1.BE33 PCH_TBT PERST# → FREE	0.1(x00)
26	17,18	2018/07/23	3.3V_CAM_EN# change, TAT_RTD3_WAKE# reserve	1. 3.3V CAM EN# contact to FCH GPP D2(pin BE18) 2. Reserve Oohm for TBT RTD3 WAKE# to PCH GPD7(pin BE41) add RC834,RH662@,RH663 change name RH602.1 TBT RTD3 WAKE# GPD7 change name RH661.2 TBT_RTD3_WAKE#_K18	0.1(x00)
c 27	58	2018/07/24	remove EC VTR3 3V3 power jump	1.remove PJP21 2.+1.8V 3.3V ALW VTR3 → +1.8V ALW VTR3	0.1(X00) _c
28	44	2018/07/24	Vendor review,PD cc cap value change	CT85,CT86 470pF 220pF RT98 0 ohm 100k ohm	0.1(X00)
29	12	2018/07/25	VCCPLL bead stuff	VCCPLL LC562 stuff,RC422 unstuff	0.1(X00)
30	16	2018/07/25	ESD reserve Components	reserve CH554,CE548,CC549,CH550,CH551,CH552,CC556,CH553,DA9,DA10,DZ13,CC557,CC558	0.1(X00)
31	17	2018/07/26	follow NB ROM part change	1/UC5 VPRO use SA00009RI10 2/UC5 NVPRO use SA00003X910 3.UC6 NVPRO use SA00005VV20	0.1(X00)
32	38	2018/07/31	EMI change choke size	LZ1,LIZ(LI3,LI4) SM070005U00	0.1(X00)
33	12	2018/07/31	power name change	1.+VCC_CORE - LA CORE 2.+VCC_GT - 4GT_CORE 3.+VCC_SA - +SA_CORE	0.1(X00)
3 4	9	2018/08/03	change DDI port	1. (DDI1) HDMI→ AR R3 2. (DDI2) AR PO→ AR P1 3. (DDI3) AR P1→ AR P2	0.1(X00)
35	44	2018/08/08	Change PD controller to 65982DD	Change UT5 part to SA0000C8000 from SA0000BIJ00.	0.1(X00)
36	66	2018/08/08	Change ST TPM to ST33HTPH2032AHC1	Change UZ12 part to SA0000C5G10 from SA00009SO40.	0.1(X00)
37	16	2018/08/10	follow CFL H PDG 24MHZ topology	remove RH437,direct connect	0.1(X00)
38	62	2018/08/14	follow NB M_BIST schematic	1.DZ12,RZ1413 unstuff 2.add RZ1482(M_BIST_R) PU +3.3V_ALW 3.CZ218 change to 2.2uF	0.1(X00)
39	17	2018/08/14	not support KBL H	remove RH171	0.1(X00)
40	56	2018/08/14	codec bom modify follow NB	RA53 stuff,RA54 unstuff	0.1(X00)
41	17	2018/08/14	WWAN_PWR_EN connect to PCH	1.WWAN_PWR_EN need connect to PCH pin GPP_D0 2.WWAN_PWR_EN change net name to WWAN_FULL_PWR_EN	0.1(X00)
42	14	2018/08/14	CNVI PDG update	RZ1382,RZ1384 change to 33 ohm,close to PCH	0.1(X00)
_A 43	52	2018/08/22	naming change	1.+TS_PWR_SRC	
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44	44	2019708722	follow compal naming rule	TBTA_TOP P SW_TBT_A_USB20_P2 TBTA_TOP N SW_TBT_A_USB20_N2 TBTA_BOT_P SW_TBT_A_USB20_P1 TBTA_BOT_N SW_TBT_A_USB20_N1 TBTA_TOP_P R SW_TBT_A_USB20_P2_R TBTA_TOP_N_R SW_TBT_A_USB20_N2_R TBTA_BOT_P R SW_TBT_A_USB20_P1_R TBTA_BOT_P R SW_TBT_A_USB20_P1_R TBTA_BOT_N_R SW_TBT_A_USB20_N1_R	0.1(x00)	
45	52	2018/08/28	implement support 7360 card schematic	1.add component RZ1397,QZ19,RZ1398,RZ1399,UZ51,CZ216,RZ1395,RZ1396,RZ1394,RZ1403,RZ1404,CZ217,RZ1406 RZ1401,RZ1481,RZ1480,RZ1402,RZ1405,RZ1400,RZ1393,RZ1450,RE340,RC840,RC756,UZ52 2.JNGFF2.54 PCIE WAKE# — WWAN PEWAKE# 3.JNGFF2.67 NC — WWAN_BB_RST# 4.UE1.K1 NC — WWAN_GPIO_CTRL add GPIO UH1.BC17 — WWAN_GPIO_PERST# UH1.BF35 — WWAN_BB_RST# UH1.BF35 — WWAN_GPIO_WAKE#	0.1(x00)	
46	58	2018/08/30	allign NB modify schematic	1.reserve RE821 SSD SCP# PU to +3.3V_ALW 2.WWAN reserve RZ1484,RZ375 PU 3.reserve CN77 22U for support Teton Glacier in the future	0.1(X00)	
47	54	2018/08/30	HW internal review	1.UT11.22 UT12.22 PWD pin add test point for test 2.UZ5 remove?need HW meeting discuss 3.VCCST_PWRGD not need connect to EC,remove RE308,RE552,UE1.K10 change name to SLP_WLAN#_GATE 4.WEC_ACTIVITY_STATUS# not need connect EC to USH connect,UE1.E4 change name to VOI IN3# 5.RE401 stuff for RTC_DET# PU to +1.8V_ALW_VTR3 6 not use/LPC,remove PCH PLTRST# EC net,remove RH244,RE375 7.remove RE560,ESPI_RESET# direct connect to JESPI 8.remove DZ7,RZ87,USH DET# direct connect to JESPI 9.remove NVME_LED#_SATALED#,RN100,RH380,RN101 10.for reduce nower consumption,stuff RN227 11.UZ23,CZ129,CZ130 unstuff for reserve 12.JUSB2,JUSB3 VBUS add 150uF CI103,CT104 13.change name TP_DISABLE#_PTP_DISABLE#_R- PTP_DISABLE#R 14.for S3 no power legge not use,remove QZ4,RZ370 15.allign NB,RZ1484 stuff RZ379 unstuff,RZ375 remove 16.remove RV1652,CV1639,name change DGPU_PWR_EN_RC- DGPU_PWR_EN_D 17.remove QV24,RV667	0.1(x00)	
48	52	2018/09/03	WWAN_GPIO_PERST# PU power change	RZ1405 PU change to +3.3V_RUN unstaff add RZ1485 PU change to +3.3V_RUN unstaff	0.1(X00)	
49	52	2018/09/04	GPIO name change	1.HDD_EN_PCH → PCH_HDD_EN	0.1(X00)	
50	68	2018/09/04	support optane SSD add cap	1.CN60 68P_0402 change to 0.01u_0402 2.add CN80,CN81,CN84,CN82 0.01u_0402 3.add CN86 0.1u_0402	0.1(X00)	
51	18	2018/09/04	PDG eSPI series resistance update	RC366,RC367,RC368,RC369 change to 0 ohm RH97 change to 33 ohm	0.1(X00)	
52	56	2018/09/04	Space limitation, remove audio load SW	remove UZ5,PJP15,PJP16,CZ125,CZ126,CZ127,CZ128 RH345 change to @	0.1(X00)	
53	15	2018/09/05	save layout space	delete:T37,T38,RH60,RH375,RE547,RL70 downsize to 0201:RH65,RH187,CC32,RH133,RH132,RH10,RH11,RH13,RH14,RH15,RH16,RH17,RH30 RH316,RH378,RH348,RH350,RH441,RH203,RH204,RH424,RH309 change to test point:RH99(T424) DELL CONFIDENTIAL PROPE Compal Electronics, In PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DAMNING AND SPECIFICATIONS CONTAINS CONTIDENTIAL THADE SECRET AND OTHER PROPRIETARY INFORMATION OF BELL INC. ("DELL") THIS DOCUMENT MAY NOT EE P.I.R	IETARY	
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54	52	2019/09/14	follow NB change resistance value	RZ1405,RZ1485,RC756 change to 10k_0201	0.1(X00)
55	21	2018/09//1/9/	KBL WHEA issue,intel recommend add fillter	Stuff LH421, CH349, CH45 and no stuff RH238 to LC for 1.0V_XTAL	0.1(X00)
56	38	2018/09/20	FUSE change to stuff	1.RZ1387 → FZ1(SP04007G00) 2.RV103 → FV1(SP040007G00) 3.RZ90 → FZ2(SP040007G00) 4.RZ98 → FZ3(SP040007G00) 15HD:remove PJP13 15HU:remove PJP13	0.1(x00)
57	58	2018/09/20	follow GPT0 table	UE1.K7 RTC_DET#,RE401 remove PCH_GPP_D3:Reserved RTC_DET# for factory test only,add RC401 PU	0.1(X00)
58	58	2018/10/02	add GPIO for smokeless	add UE1.D6 CPU_OVP remove RE731	0.1(X00)
59	58	2018/11/12	FPR_SCAN_INT# leakage when no instal FPBTN module	add MOS QE20 add FPR SCAN_INT# PU RE826(10K) +3.3V_FPBTN add FPR_SCAN_INT# EC RE827(10K)PU +3.3V_ALW remove RE709(100K) reserve RE825(0 ohm) UE1.L8 change name FPR_SCAN_INT# → FPR_SCAN_INT#_EC RZ144.1 change name FPR_SCAN_INT# → FPR_SCAN_INT#_EC RZ114.2 change name FPR_SCAN_INT# R → FPR_SCAN_INT#_EC	0.2(X01)
60	18	2018/11/16	align NB	RH661 from 1K change to 10K	0.2(X01)
61	42	2018/11/16	align NB TBT RTD3 schematic	reserve RTD3 0 ohm(RT554,RT555)	0.2(X01)
62	45	2018/11/16	PD use Internal LDO,depop unuse parts	depcp UT8,CT94,DT3,CT93,DT1,DT2,RT393,CT89,RT111,CT90,UT7,CT91	0.2(X01)
63	21	2018/11/16	align NB pop bead,cap	pop LH423,CH350,CH324 Sepop RH289	0.2(X01)
64	67	2018/11/19	For save consumption,reserve SATA repeater PD pin to SO	reserve DN1 DN1.1 connect to SIO_SLP_SO# DN1.2 connect to NDD_UN7_EN_R	0.2(X01)
65	7	2018/11/21	EMC request reserve 0 ohm on XDP trace	1) PCH_RSMRSI#_AND,RC841 2) SIO_PWRBTN#, RC842 3) PCH_JTAG_TCK, RC843 4) CPU_XDP_TRST#, RC844 5) DDR_XDP_WAN_SMBCLK, RC845 6) DDR_XDP_WAN_SMBDAT, RC846	0.2(X01)
66	58	2018/11/21	EMC request add diode	1. RUN_ON_EC: add diode SC40000808 (DE43) 2. DDR4_Dramrst#_PCH: add diode Sc40008DS00 (DD32)	0.2(X01)
67	52	2018/11/21	RF request change to use bead	1.LI9 depop 2.RI49,RI50 change to use SM01000TP00	0.2(X01)
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68	62	2019/01/03	DFX request	15" add Fiducial Mark FD8	0.3(X02)	
69	52	2019/01/03	RF BOM option	1.LI9 depop 2.RI49,RI50 change to use SM01000TP00 3.RI49,RI50 change name to LI49,LI50	0.3(x02)	
70	58	2019/01/03	reserve the CNVi detect on GPP_D20	1.remove test point T269 2.reserve 0 ohm RE828 3.RE828.1 CNVI_EN# connect to PCH GPP_D20 4.RE828.2 connect to CNV DET#_EC 5.CNVI_EN# reserve 75K PD (RH868)	0.3(x02)	
71	52	2019/01/03	INTEL suggest REF LK CAV need impendence control	1.remove 0 ohm RZ371,RZ81 2.remove net ISH_UART0_RXD,ISH_UART0_TXD,ISH_UART0_CTS#,ISH_UART0_RTS#	0.3(x02)	
72	56	2019/01/03	DFX request	DA4,DA5 change footprint to 1N4148WS-7-F_SOD323-2	0.3(X02)	
73	59	2019/01/03	board ID change to X02	board ID RE79 change to X02 62K ohm	0.3(X02)	
74	38	2019/01/03	align NB reserve fuse	1.reserve FZ4,FZ5,RZ1486 2.add RZ1487,RZ1488 0 ohm	0.3(x02)	
75	23,24	2019/01/03	DFX request	JDIMM1,JDIMM2 change footprint to FOX_ASAA821-H4RB5-7H_260P	0.3(X02)	
76	38	2019/01/03	to avoid camera & DMIC lost after ESD test	pot DA9,DA10	0.3(X02)	
77		2019/01/03	0 ohm change to short pad	location reference X10 BH DVT2.0 0 Ohm_190104.xlsx	0.3(X02)	
78	66	2019/01/03	align LKE reserve TPM power source	+3.3V_VPS_UZ12/reserve 0 ohm RZ1489 to +3.3V_ALW	0.3(X02)	
79	38,58	2019/01/03	ESD request	reserve cap (1u touch screen pd# r (cvin3) cam mīc_cbl Det# (vvi12) bia_pwm (cvi11) cpf hpd (cvi10) touch screen Det# (cvi09) ir cam Det# (cz1203) ce548 from 0.1u 0201 change to 4700p 0402	0.3(x02)	
80	7,38	2019/01/03	ESD request	CC306,CC308,CC302,CH551,CC305,CC304,CC303,CV113,CV112,CV110,CV109,CZ1203 from reserv to add 0.1uF cap CE548 from 47nF reserve to add 47nF	e0.3(X02)	
81	7,18	2019/01/03	ESD request	RC124 depop,CC307 100pf pop CH266 100 pf POP	0.3(X02)	
82	52	2019/01/03	BOM option for non WWAN SKU	HU non WWAN SKU BOM option 1.L18,L116,L117,C2198,C242,C241,C223~C226 change to WWANRF8 2.U229,C2154,C2155,R2360,C2150,C2151,C2152,C2153,C210,C211(R243,D25,D26,C237,R21406,C2217,U252,R21405,R21400,U251,C2216,Q219,R21399,R21397,Q28,C217~C221 change to WWANR	0.3(x02)	
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83	ALL	2019/03/06	0 ohm change to short pad	follow pilot 0 Ohm_190305 table to modify	1.0(A00)
84	18	2019/03/06	remove service mode switch for MP	depop SW1, RH101 short pad RH100	1.0(A00)
85	59	2019/03/0	board ID change	RE79 change to 4.3k	1.0(A00)
86	ALL	2019/03/06	DFX request, add green paint	footprint add "-NPM" 15HD:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29, RI30,CI104,RZ96,RH289,LI11,LI12,LI13,CI103	1.0(A00)
				15HU:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30,CI104,RZ96,RZ108,RZ102	
				14HD:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30, CI104,CI103,CI32	
				14HU:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29, RI30,CI104,RH289,CI103,CI32,CI104	
87	52	2019/03/06	Align NB schematic	Change RZ43 from 47K_0402_5% to 10K_0402_5%	1.0(A00)
88	51	2019/03/06	DFB suggest modify UL1 pad layout dimension to 6 6 6.6mm	UL1 change footprint to WGI219LM-SLKJ3-A0_QFN48_6X6	1.0(A00)
89	52	2019/03/06	align NB change UZ52 power rail from 3.3V_RUN to 3.3V_ALW	RZ1403 depop,RZ1404 pop and keep 0 ohm	1.0(A00)
B		5		THORSEEAN NOTE: THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUE CONTINUE CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN THE SHEET OF BUILDERING DAMAGE AND SECUTION CONTINUES. IN SHEET DAMAGE AND SECUTION CONTINUES. IN SHEET DAMAGE AND SH	Rev 0.2

